

Module Specification
for
intcon

Revision 1.6

February 9, 2002

Contents

1 Document Information **3**
1.1 Scope . . . 3
1.2 Trademarks . . . 3
1.3 Related Documents . . . 3

2 Module Level Specification **4**
2.1 Architecture & Functional Description . . . 4
2.1.1 Operation . . . 4
2.2 Claims & Assumptions . . . 4
2.3 I/O Description . . . 4
2.4 Design Guidelines & Exceptions . . . 5
2.5 Block Diagram . . . 5
2.6 Register Map . . . 5
2.6.1 Interrupt Mask Register . . . 5
2.6.2 Interrupt Priority Register . . . 6
2.6.3 Interrupt Request Register . . . 6
2.7 Timing diagrams . . . 7
2.8 Timing specification & Performance . . . 8
2.9 Power Dissipation . . . 8
2.10 Size & Gate Count . . . 8
2.11 Test Structures, Testability & Test Coverage . . . 8
2.12 Configuration Information & Parameters . . . 8
2.13 Recommended Clocking & Reset Strategies . . . 8
2.14 Recommended System Verification Strategy . . . 9
2.15 Recommended Test Strategy . . . 9
2.16 Floorplanning Guidelines . . . 9
2.17 Debug Strategy . . . 9
2.18 Version History & Known Bugs . . . 10

1 Document Information

1.1 Scope

The scope of this document is limited to the technical specification of the intcon module, used in the Indus System-On-Chip (SOC) device. Shera Technology Corporation reserve the right to modify this specification without notice.

This document is maintained by Shera Technology Corporation (Taiwan).

1.2 Trademarks

The WISHBONE System-On-Chip Interconnection Architecture for Portable IP Cores Rev B.2, is an open IP core interconnection standard which is developed and maintained by the Silicore Corporation (USA).

Indus is a trademark of Shera Technology Corporation (Taiwan).

1.3 Related Documents

TBD

2 Module Level Specification

2.1 Architecture & Functional Description

The Indus interrupt controller generates the lightfoot interrupt and vector. It accepts inputs from up to 32 peripheral interrupt sources.

The interrupt controller is connected to the Register Extension Bus.

2.1.1 Operation

The 32 interrupt sources are masked with the contents of the 32-bit Interrupt Mask Register (IMR). Each masked interrupt is used as the enable signal for a 4 to 16 bit one-hot encoder.

The input to the 32 one-hot encoders is the contents of the 128-bit Interrupt Priority Register (IPR).

The 32 16-bit one-hot priority signals are ORed together to form the input to the interrupt controller's Priority Encoder. When any of the 16 priority encoder inputs is high a lightfoot interrupt will be generated.

The interrupt vector produced depends on which of the 16 input bits is high, in the case of multiple input bits being high, the input with the highest prioirity sets the vector.

The status of the 32 interrupt sources (pre-masking) can be read by reading from the IRQ register.

2.2 Claims & Assumptions

TBD

2.3 I/O Description

Figure 1.

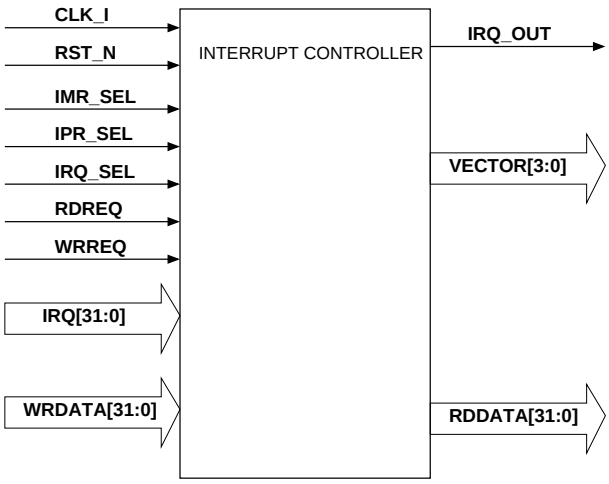

Figure 1: Interface

All module interface signals are described in Table 1

Signal Name	Type	Active Level	Description
clk	clock	high	System Clock
rst_n	reset	low	System Reset
imr_sel	input	high	Interrupt Mask Register Select
ipr_sel	input	high	Interrupt Priority Register Select
irq_sel	input	high	Interrupt Request Register Select
wrdata[31:0]	input	high	Register Bus Data In
wrreq	input	high	Register Bus Write Request
rdreq	input	high	Register Bus Read Request
irq[31:0]	input	high	Interrupt Sources
irq_out	output	high	Lightfoot Interrupt
irq_vector[3:0]	output	high	Lightfoot Interrupt Vector
rddata[31:0]	output	high	Register Bus Data Out

Table 1: Module Interface Signal Description

2.4 Design Guidelines & Exceptions

TBD

2.5 Block Diagram

TBD

2.6 Register Map

All module registers are described in Table 2.

Register	Type	Select Lines			Width (Bits)	Description
		irq	ipr	imr		
IMR	Read-Write	0	0	1	32	Interrupt Mask Register
IPR	Write-Only	0	1	0	128	Interrupt Priority Register
IRQ	Read Only	1	0	0	32	Interrupt Request Register

Table 2: Module Register Description

Each register is described in more detail in the following subections.

2.6.1 Interrupt Mask Register

The register bits are described in Table 3.

Mask[31:0]
Interrupt Mask Bits

Table 3: Interrupt Mask Register

Mask Bits 31:0 The Mask bits are ANDed with the 32 interrupts to mask possible interrupt sources. When set high an interrupt will be unmasked. When set low an interrupt will be masked. The Mask Register is set low on sytem reset.

2.6.2 Interrupt Priority Register

The register bits are described in Table 4.

127:124	123:120	119:116	115:112	111:108	107:104	103:100	99:96
IRQ[31]	IRQ[30]	IRQ[29]	IRQ[28]	IRQ[27]	IRQ[26]	IRQ[25]	IRQ[24]

95:92	91:88	87:84	83:80	79:76	75:72	71:68	67:64
IRQ[23]	IRQ[22]	IRQ[21]	IRQ[20]	IRQ[19]	IRQ[18]	IRQ[17]	IRQ[16]

63:60	59:56	55:52	51:48	47:44	43:40	39:36	35:32
IRQ[15]	IRQ[14]	IRQ[13]	IRQ[12]	IRQ[11]	IRQ[10]	IRQ[9]	IRQ[8]

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
IRQ[7]	IRQ[6]	IRQ[5]	IRQ[4]	IRQ[3]	IRQ[2]	IRQ[1]	IRQ[0]

Table 4: Interrupt Priority Register

Priority Bits [4N+3:4N] Each interrupt source has an associated priority stored as a 4-bit value in the Interrupt prioirity register. The bits of the priority register are set in the following manner:

The 4-bit priority value is placed in byte 0 of a word. Byte 1 is loaded with the interrupt source to be programmed. This word is then written to the interrrupt priority register. The interrupt source address is decoded and the 4-bit priority is written to the appropriate 4 bits of the 128-bit interrupt priority register.

All bits of the Interrupt Priority Register are set low on system reset. This register is write-only.

Bit[31:16]	Bit[15:8]	Bit[7:4]	Bit[3:0]
Reserved	Interrupt Source	Reserved	Interrupt Priority

Table 5: Loading the Interrupt Priority Register

2.6.3 Interrupt Request Register

The register bits are described in Table 6.

Bit31:0
IRQ [31:0]

Table 6: Interrupt Request Register

IRQ Source 31:0 The interrupt controller has 32 possible interrupt source inputs but only 16 interrupt priorities. It is therefore possible that multiple interrupt sources may be assigned the same priority. In order for the interrupt service routine to determine which interrupt source interrupted the lightfoot core the value

of the 32 interrupt sources pre-mask can be MUXed onto the register read data bus. Reading from the IRQ reg achieves this.

2.7 Timing diagrams

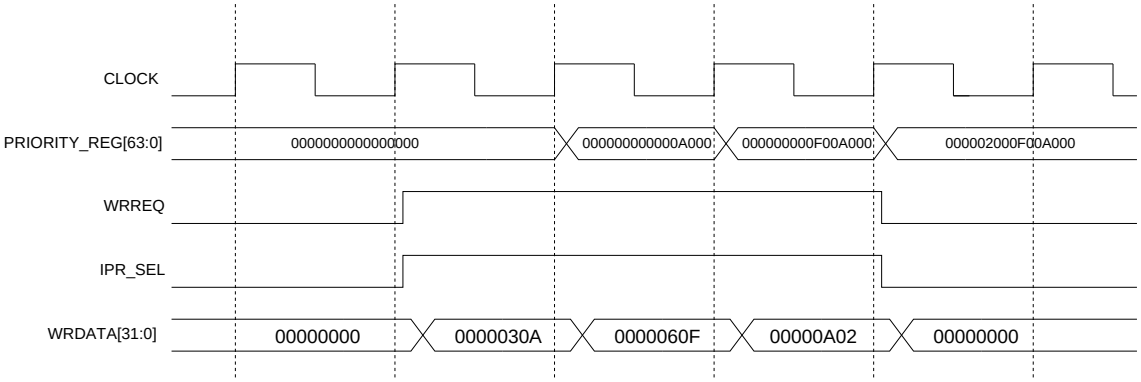

Figure 2: Interrupt Priority Register Write Timing

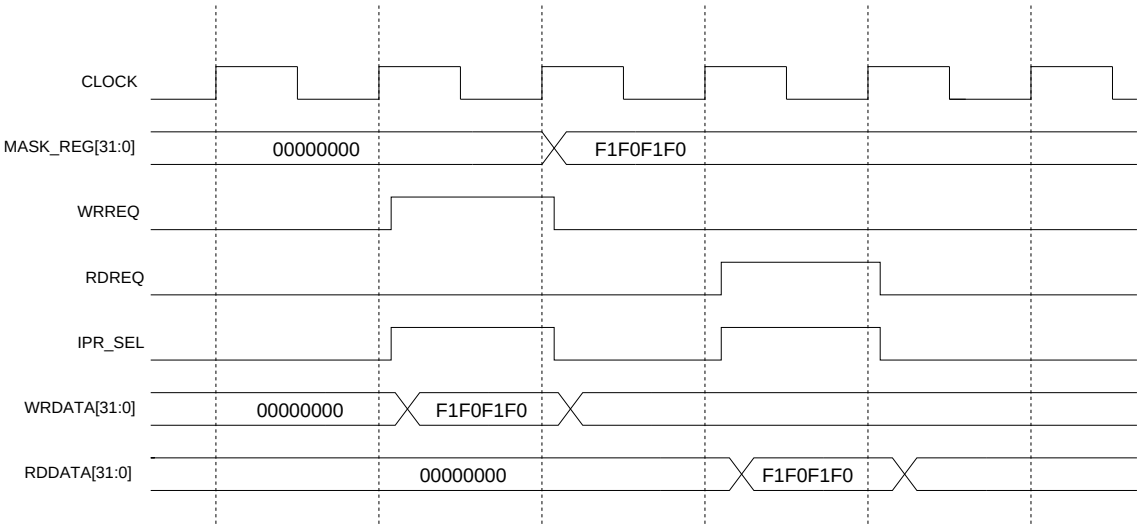

Figure 3: Interrupt Mask Register Read/Write Timing

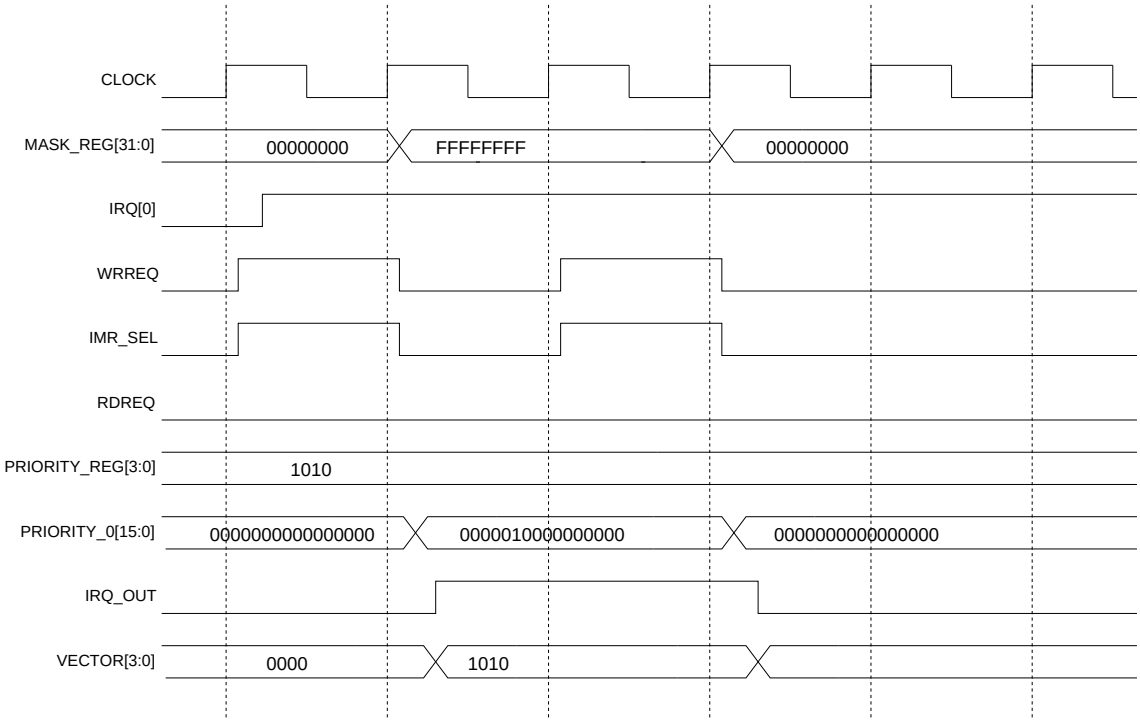

Figure 4: Interrupt IRQ in - IRQ out

2.8 Timing specification & Performance

TBD

2.9 Power Dissipation

TBD

2.10 Size & Gate Count

TBD

2.11 Test Structures, Testability & Test Coverage

TBD

2.12 Configuration Information & Parameters

TBD

2.13 Recommended Clocking & Reset Strategies

TBD

2.14 Recommended System Verification Strategy

TBD

2.15 Recommended Test Strategy

TBD

2.16 Floorplanning Guidelines

TBD

2.17 Debug Strategy

2.18 Version History & Known Bugs

Author	Graham Cunningham		
Date	April 10, 2002		
Current Revision	1.6		
Revision History	1.6	February 9, 2002	IRQ in-out Timing Diagram Added
	1.5	February 5, 2002	Timing Diagrams Added
	1.4	February 1, 2002	First Draft of Documentation
	1.3	January 31, 2002	Server Change mid project