verilog2vhdl™ Release Notes

Software Version 6.0

May 2007

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Use these Release Notes in conjunction with the **verilog2vhdl** User's Manual, which describes the installation and basic operation of the tool.

General questions and inquiries can be sent to:

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Changes in current version (6.0)

1. Added ‘pragma translate_on’ and ‘pragma translate_off’ to the list of synthesis directives, in addition to the existing one(BZ 10)
2. Added a new switch –no_header. This switch will not print a header in the output file.
3. Made enhancements to the comment placement, to make output file similar to input.

4. Enhanced documentation. New documents added include- quick start guide, a summary of known bugs and workarounds, a brief document on recommended modeling style.

Changes in version 5.6

1. Improved Verilog pre-processor. It can process Verilog file with unlimited size. It is now able to process "defines" with empty macro.

2. The readability of the VHDL output is dramatically improved. The improvements includes proper indentation, better comment positioning, and consistent spacing between statements.

3. The unnecessary type conversion functions are eliminated. The previous version of the tool widely used type conversion functions. In some situations, these type conversion functions are not necessary, although they don't affect the functionality of the output. These unnecessary type conversion functions are eliminated in the new release so that the output code is functional and clean.

4. Shift operations and condition operations in parameter declarations are now supported.

5. License utility is upgrade in this version. The license daemon and utility distributed with the new release is version 8.2.

Changes in version 5.5

1. A new option, "-vpp", is added for integrating Verilog pre-processing. When set, this option instruct the translator to pre-process the Verilog source file, elaborate compiler directives such as "ifdef", "include", etc, and generate an Intermediate File (IF). The translation then proceeds on the intermediate file.

2. A new option, "-an", is added to allow users to rename the generated VHDL architecture. The default name of the generate architecture is "VeriArch".

3. The library name for the packages provided by ASC is renamed. The original name was "Verilog". The new name is "ASC".

4. Indentation of the output VHDL code is improved.

5. Library files provided with the translator are revised and upgraded.

Changes in version 5.0

1. The option “-mrv” is re-defined. This option improves the translation of blocking statement without putting “wait for 0 ns” after each translated statement.

2. Verilog POSEDGE/NGEDGE event controls are translated into standard VHDL edge functions : rising_edge/falling_edge, instead of the functions provided by the tool. It increases the compatibility and synthesizability of the translated code.

3. A bug in provided library files is fixed.

4. A bug in translating definition of variables is fixed.

Changes in version 4.4

1. The distributed package now includes both VHDL2Verilog and verilog2vhdl translator. They are licensed separately.

2. Using signals as delay parameters is supported.

3. A bug in Verilog for-loop is fixed. The translation could be wrong when increment of for-loop is other than 1.

4. A bug on type conversion function is fixed.

5. More ternary functions are added to the library file functions.vhd.

6. A bug in Verilog if-else statement is fixed. The sequence of translated VHDL elsif could be wrong in some cases.

7. Support of test bench translation is improved. A few bugs on FILE I/O translation are fixed.

Changes in version 4.3

1. Case statements with constant expressions are supported. In Verilog, it is possible to use a constant expression for case expression and match the value of the constant expression against case items, while it is not allowed in VHDL.

2. The **defparam** statements will not be validated if option "-nc" is used. It will allow user to continue the translation without error even if some instance modules are not available.

3. More functions are added to the library file utils.vhd.

4. A few bugs are fixed.

Changes in version 4.2

1. ASC's products now use FLEXlm License Manager.

2. The **verilog2vhdl** and **VHDL2verilog** are now two features of one ASC tool -- V2V translator. The directory structure of V2V translator is different from the old **verilog2vhdl** or **VHDL2verilog** structures.

3. The environment variables $V2V_HOME and $VHDL2V_HOME (for **VHDL2verilog** translator) are merged into a new environment variable $ASC_HOME.

4. Y2K compliant.

5. Improved Verilog pre-processor(vpp) to provide better support for 'define, 'include and 'ifdefs/ifndefs.

Changes in version 3.3 :

1. **verilog2vhdl** translator now uses Elan License Manager.

2. Two versions of *buffers.vhd* package - for synthesis and simulation - were merged into one.

3. New `-Map_Registers_to_Variables` (-mrv) switch allows to translate Verilog registers to VHDL variables. By default, registers are translated to signals. Existing restrictions on using `-mrv` switch:
   - All parameters to tasks/functions have to be passed explicitly
   - All inout/output task enabling arguments have to match the respective declared task arguments by size
   - Concatenations as inout/output parameters to tasks and functions are not supported

4. A beta-version of a Verilog pre-processor (vpp) is included in *$V2V_HOME/bin*. This pre-processor is built using the GNU gcc. 'vpp' fully supports `defines, `includes, and `ifdefs/ifndefs. Usage is `vpp input_file [output_file]`. If no output file is specified, output goes to stdout.

   Suggested usage:

   ```
   vpp input_file.v temporary_file.v
   v2v temporary_file.v temporary_file.hdl [v2v switches]
   ```

5. Instance names of Verilog primitive gates are preserved as the equivalent assignments' labels.

6. TERNARY functions in *functions*.vhd* packages were modified to comport with the behavior of the ? operator for X and Z values of the conditional expression, as defined in Verilog LRM.

7. Support for translation to VHDL std_ulogic types was removed. Now, only std_logic types are supported.

8. Support for ranges in parameter declarations was added.

9. A switch `-Preserve_order` to keep the order of concurrent statements the same as it was in the input Verilog file was added.

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Changes in current version (6.0)

1. Added ‘pragma translate_on’ and ‘pragma translate_off’ to the list of synthesis directives, in addition to the existing one(BZ 10)
2. Added a new switch –no_header. This switch will not print a header in the output file.
3. Added a new switch –no_timescale. This switch prevents printing of the timescale directive to the output.
4. Fixed issues while translating integer generics (BZ32).

5. Made enhancements to the comment placement. The translstor now a does a better job of placing comments in the output file. Added newline characters to make output look better.
6. Enhanced existing documentation and added new documents. These include- quick start guide, a summary of known bugs and workarounds, a brief document on recommended modeling style.

Changes in Version (5.6):

1. more flip-flop templates are supported. New templates include flip-flop with 2 "reset" or 2 "set" controls, and complex gated clock templates.

2. Translation without packages is now supported. The previous version stopped if any of the packages used in the design is not available. The new version will continue the translation and give a warning about the missing package, as long as missing the content of the package does not prevent the tool from running.

3. A new option, "-Force_If_Generate" (-fig), is added. With the option turned on, the tool will translate the "IF_GENERATE" block even though the "IF_CONDITION" is false. The result may need manual adjustment before compile when this option is used.

4. A new option, "-BLocking" (-bl), is added. this option tells the tool to use blocking assignments in all combinational procedural blocks. It is consistent with one of the Verilog code rules that are used by core developers.

5. A number of Space (" "), instead of Tab ("\t"), is now used in the output files for indentation.

6. License utility is upgrade in this version. The license daemon and utility distributed with the new release is version 8.2.

7. A bug in translation of VHDL "range" is fixed. In some rare cases, the attribute in range expression got dropped.

Changes in Version 5.5:

1. Accurate translation of VHDL aggregates is fully supported. The tool can automatically determine proper range and element associations.

2. 2D array access functions generated by the tools are improved.

3. Translation of vector slicing is improved.

4. Parameterization of the translation result is improved. Constants(parameters) are kept and used as much as possible, rather than elaborated.

5. 2 more forms of Flip-Flop descriptions are recognized and translated. Both POSEDGE and NEGEDGE in one condition expression is supported.

6. More complete translation log information is provided. File names and line numbers of warnings messages and errors are given in the messages.

7. Using the same enumerate elements in different enumerate type definitions is supported, although it is not recommended for translatable VHDL coding style.

8. Empty packages containing only comments will not be generated.

9. The option "-ssb" is renamed to "-tsb".

10. The option "-ssc" is set as default. A new option "-isc" is added to turn off the "-ssc" option.

11. The option "-sir" is set by default. A new option "-iir" is added to turn off the "-sir" option.

12. A new option., "-flc", is added. It will instruct the translator to generate output file in lower case.

13. A number of bug fixes, including:

    - Integer unnecessarily converting to bits
    - Not generating synthesizable code when 2D array is initialized at declaration
    - parameters from a package positioning improperly
    - problem when the size of an aggregate is zero
    - Verilog loop variable not declared sometimes because of the case sensitivity of Verilog

Changes in version 5.0:

1. The number of package files created by the tool is minimized. In old versions, the tool creates a package file for subprograms even though the subprograms are not translated automatically by the tool.

2. Package files that are created by the tool are no longer placed in the current working directory. They are now placed into the directory where the main output file is in. The user can specify the path for the directory with the output file name.

3. The VHDL attribute **'event** is now fully supported. In old versions, it can only be translated when it is used to describe a flip-flip in certain templates. More flip-flop templates and latch templates have been added to support the translation of VHDL event control. The tool now can recognize and translate more forms of

VHDL flip-flip and latch descriptions into proper Verilog flip-flop and latch syntax.

4. The VHDL attribute **'last_value** is now supported. This attribute sometimes is used to describe a flip-flop, and is often used for event control in test bench descriptions.

5. Procedure mapping is now supported in addition to function mapping. Function mapping is widely used to eliminate unnecessary VHDL type-conversion functions, or to replace them with user defined Verilog functions. With procedure mapping, you can even map VHDL procedures and system functions such as **write**, **writeline**, and **now** to proper Verilog tasks or functions. This significantly increases the tool's support of test bench related translation.

6. Verilog reserved words that are used as identifiers in VHDL files are now translated to Verilog identifiers by default. The Verilog identifiers start and end with the underscore character ("_"). The tool issues a warning message each time such an identifier is encountered so that the user can check and assure the correctness of the translation. In old versions, the tool reports an error and just stops translating.

7. Specifying integers with a range in port declaration is now supported. In old versions, integers with range are supported only when they are used in block definition.

8. Translator directives are now supported. In this version, three pairs of directives are added:
   -- **translate_off** and **translate_on**,
   -- **synopsys translate_off** and **synopsys translate_on**,
   -- **synthesis translate_off** and **synthesis translate_on**.
   The block between the directive pairs is treated as a comment.

9. A new option, **no_component_check** (ncc), is added. This option forces the translation to proceed even though some or all of the instantiated entities or components are not available, eliminating the necessity of translating the whole design at once. You can now can translate a hierarchical design one component at a time, or re-translate an individual file in the whole design without involving all the others.

10. Array aggregates are fully supported, both position association and name association. The old version just supported aggregates with only one element association.

Changes in version 4.4: :

1. Bit wise access of multi-dimensional arrays is now supported. A new switch **"-sm"** is added for this feature.

2. Integer with range is now supported. A new switch **"-sir"** is added for this feature.

3. Integer constant with based initial values are translated to parameters with proper based initial values that allow concatenation.

4. VHDL operator **"ABS"** is now supported.

5. VHDL concurrent signal assignment with register target is translated to an always block with proper sensitivity signals or an initial block.

6. VHDL operator **"**"** is supported if it is used in constant declaration.

7. Fixed a bug in VHDL physical unit translation.

8. Fixed a bug in VHDL **"wait until" statement** translation.

9. Fixed a bug in VHDL aggregation translation.

10. Fixed a bug that caused segmentation errors.

Changes in version 4.3:

1. The **VHDL2verilog** now supports VHDL alias statement. A Verilog `define will be added for each VHDL alias statement.

2. The **VHDL2verilog** now supports VHDL attribute "range".

3. VHDL generate statements can be preserved by using an option "-pg". In this case, the generate block will not be elaborated.

4. The translator now supports vector slicing. A VHDL vector, one slice of which is on the left hand side of a concurrent signal assignment, and the other slice of which is on the left hand side of a sequential signal assignment, will be translated to Verilog correctly.

5. Fixed a few bugs that caused segmentation errors.

6. Improved translation of wait statements and functions.

Changes in 4.2000 :

1. ASC's products now use FLEXlm License Manager.

2. The **VHDL2verilog** and **verilog2vhdl** are now two features of one ASC tool -- V2V translator. The directory structure of V2V translator is different from the old **VHDL2verilog** or **verilog2vhdl** structures.

3. Y2K compliant.

4. Improved support for enumerated type and multidimensional array types. The problem with the occasional wrong subscript has been fixed.

5. Fixed problem with recognizing physical units of timescale: ms, us, ps, etc.

6. Fixed problem with the bitwidth of function return values.

7. Improved translation of subprogram body.

8. The environment variables $VHDL2V_HOME and $V2V_HOME (for **verilog2vhdl** translator) are merged into a new environment variable $ASC_HOME.

Changes in version 2.8:

1. NT version of **VHDL2verilog** now uses FLEXlm License Manager.

2. A function map file option was added : **`change`**. The functionality of the `change` option is basically similar to that of the `replace` option. The difference between the two options is that `replace` will remove all arguments of the subprogram that is being replaced, while `change` will leave all arguments in place (and just change the subprogram name).

3. Improved support for `CHARACTER` and `STRING` types.

4. When subprograms are ignored during function mapping, the translator verifies if it is ok to drop the parentheses of the arguments. Otherwise the parentheses will be left in place to ensure correct elaboration.

5. Support for `RECORD` types in VHDL. The records are elaborated before translation: `<record_name>_<element_name>`

6. Improved way bitwidth expressions are printed. (No longer any expressions like: 4 - 0 + 1).

7. Fixed problem with the order of `include statements. The order was reversed which could lead to compilation problems due to inter-dependencies.

8. When using -synth switch, GENERIC MAP constructs are mapped to a synthesizable parameter value assignment of form: *module*_identifier **#(parameter_value_assignment)** module_instance

Changes in version 2.7:

1. **VHDL2verilog** now uses Elan License Manager.

2. -File <command_file> switch was added. The command file can contain input filenames, output filename, or switches (including -f switch).

3. -SYNTHesis switch was added. The purpose of the switch is to eliminate non-synthesizeble constructs from the output of the translation. The present functionality is limited to suppressing initial statements, using logical (in)equality operators in place of case (in)equality operators, and suppressing pullup and pulldown instantiations in the output.

4. -87 switch was added. Allows reading VHDL'87 files. The default is VHDL'93.

5. A utility called 'mapmaker' was added to allow easy modifications of the vhdl2v.map file. The utility scans all specified VHDL files for package declarations and makes corresponding entries in vhdl2v.map file.
   Usage: mapmaker {-d pathname} <list_of_VHDL_files>
   The -d option specifies the directory where the vhdl2v.map file is saved. All files to be scanned for packages need to specified on the command line. E.g.:
   mapmaker *.vhd *.vhdl

6. Support for simple configurations was added, which enables to select one from a series of available architectures.

7. Subprograms with unconstrained types in the interface elements are reconfigured to constrained types based on the type in the function/procedure call. This effectively creates a copy of the original subprogram for a specific combination of sizes of its parameters.

8. Two extra actions : operator and unary_operator were added to the function map file. They support direct mapping of specified functions to Verilog operators. The symbol of the target Verilog operator should be put in the Argument field (see Users' Manual).

9. Concurrent assignments with literals 'L' or 'H' on the right hand side are translated to `pulldown` or `pullup` instantiations.

10. Translation of enumerated types was improved. In this version, names of enumerated types declared locally are prefixed with the label of the owner of the block declaration. All enumerations in turn are translated into integer parameters. Names of the parameters are prefixed with the name of the corresponding enumerated type. Entities of enumerated types (signals or variables) are translated into reg's of the size to accommodate the largest enumeration of the corresponding type.

11. Support for use of constants and generics in generates was added.

12. Command line with which the tool was called is printed in the log file

13. `$VHDL2V_HOME/bin` or `$VHDL2V_HOME/lib` were made the default locations of all `.map` files

14. `'range, 'length, 'high, 'low, 'right, 'left` attributes are supported and elaborated.

15. All assignments using aggregates with `OTHERS` on the right hand side are supported except cases where:
    - the target of the assignment is an aggregate
    - other association elements are present in the RHS expression, along with OTHERS
    - only hex and octal based literals are not supported as actuals for RHS association elements

16. The VHDL ** (POWER) operator is elaborated if used in generates. In all other cases the ** operator is not translated, and a warning is printed.

17. Multiple input files are supported. The translation of all input files is written into one output file. It is required that a file name is specified on the command line for translation of multiple input files.

18. Subprogram calls are supported. Subprogram body templates are written out in a separate file `<entity_name>_<architecture_name>.verilog` which is included in the translation of the main design. Subprogram bodies have to be manually translated.

19. Simulation time is now printed for every VHDL `ASSERT` statement.

20. Instantiation of components with ports different from those of corresponding entities is supported. Component instantiation port maps are always printed as by-name maps, even in cases when the original instantiation used map-by-order. The

primary reason for such translation is to remove ambiguity in port mapping for components with ports different from respective entities. In cases when no entity is available for a component, port mapping style (by order or by name) of the VHDL instantiation is preserved in the translation.

Previously, the translator always preserved the port mapping style of the input VHDL design which created syntax errors in the output for specific components (see above).

21. With `-Include_Packages` switch, translation of package components is written out into a file *_modules.verilog. This file is included in the main output file. Previously, translation of components was written into the main output file regardless of the `-Include_Packages` switch.

22. Support for translation of an entity without an architecture REMOVED. For this case, no output is produced.

23. VHDL `GENERATE` statements are supported