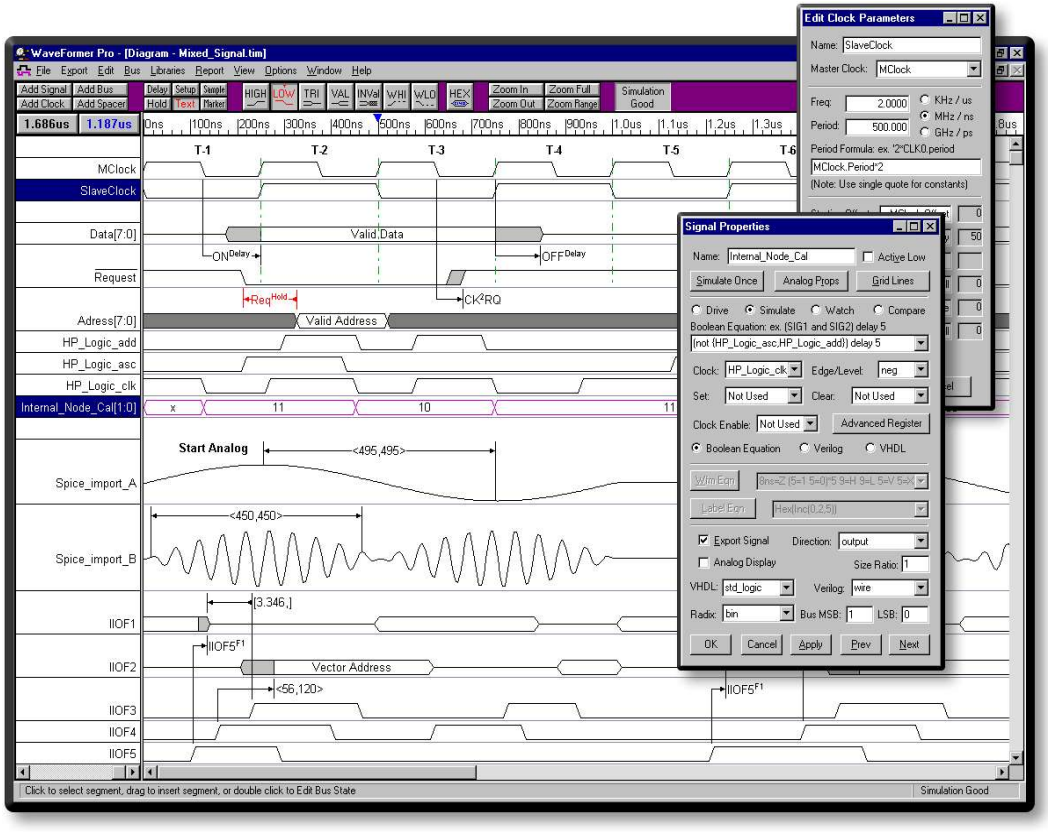
Reactive Test Bench Generation



An option that generates VHDL and Verilog test benches that react to the simulation model!

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Non-Reactive Test Benches

- **Non-Reactive Test Bench Benefits:**
  - Free with WaveFormer Pro, VeriLogger Pro, and DataSheet Pro
  - Generates VHDL and Verilog stimulus models and test benches from graphical timing diagrams based on absolute time
  - Auto-extracts port information from MUT into diagram
  - Instantiates MUT inside of test harness
- **Problems:**
  - Does not address generating clocked stimulus
  - Does not address the problem of figuring out if the results from the MUT are correct
  - Does not allow insertion of user defined code
  - Drawing complex waveforms can be tedious since looping constructs don't exist

Unclocked Stimulus

Without the RTB option, stimulus is *unclocked*, so time delay values control when stimulus is driven

VHDL:

```
wait for 50 ns;
SIG0 <= '0';
wait for 50 ns;
SIG1 <= '0';
```

Verilog:

```
#50;
  SIG0_driver <= 1'b0;
#50;
  SIG1_driver <= 1'b0;
```

RTB adds Clocked Stimulus

With RTB, signal stimulus can optionally be *clocked* relative to one or more* clock signals

VHDL:

```
wait until rising_edge(CLK);
SIG0 <= '0';
wait until rising_edge(CLK);
SIG0 <= '1';
```

Verilog:

```
@(posedge CLK);
SIG0_driver <= 1'b0;
@(posedge CLK);
SIG0_driver <= 1'b1;
```

*Multiple clock domains create one process per clock

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Reactive Test Bench (RTB) Graphical Tool Set

- **Waveforms -** represent stimulus and expected responses
- **Variables -** store sampled values and can modify the driven stimulus vectors during a simulation run.
- **Delays -** control edge timing with min, max, typical, and random time delays
- **Setups & Holds -** monitor stability between transitions
- **Samples -** verify and react to output from MUT
- **Markers -** model looping constructs, insert native HDL subroutine calls, or end transaction

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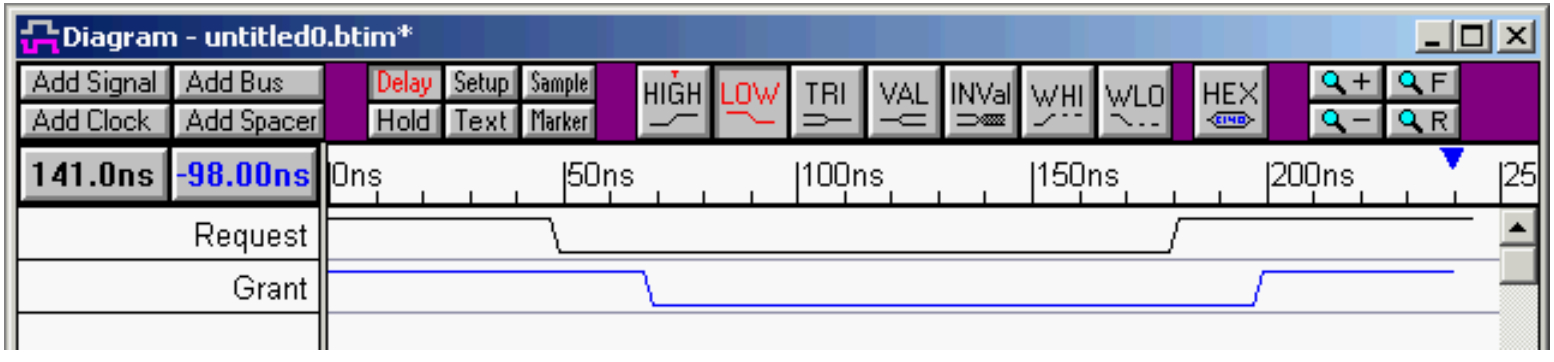
Waveforms Provide Stimulus and Expected Response Information

- Graphically draw stimulus waveforms on the input ports of the model under test.
- Graphically draw expected response waveforms on the output ports of the model under test



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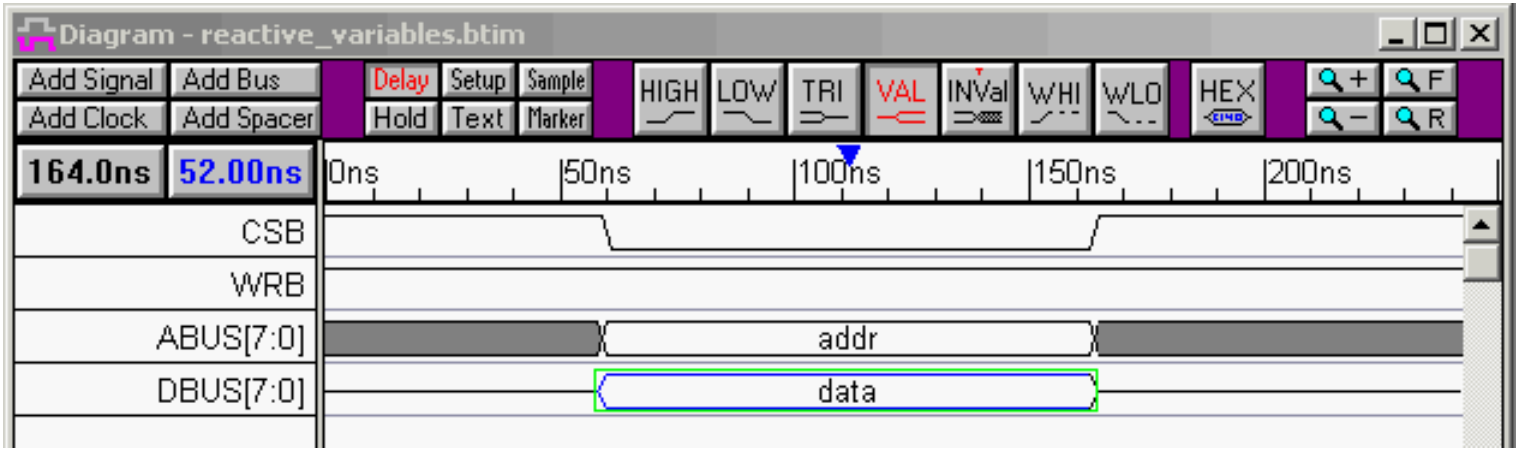
Variables Parameterize State Values

- Variables can drive values on stimulus waveforms
- Variables can store values on expected waveforms
- Waveform states can be expressed as conditional expressions using variables



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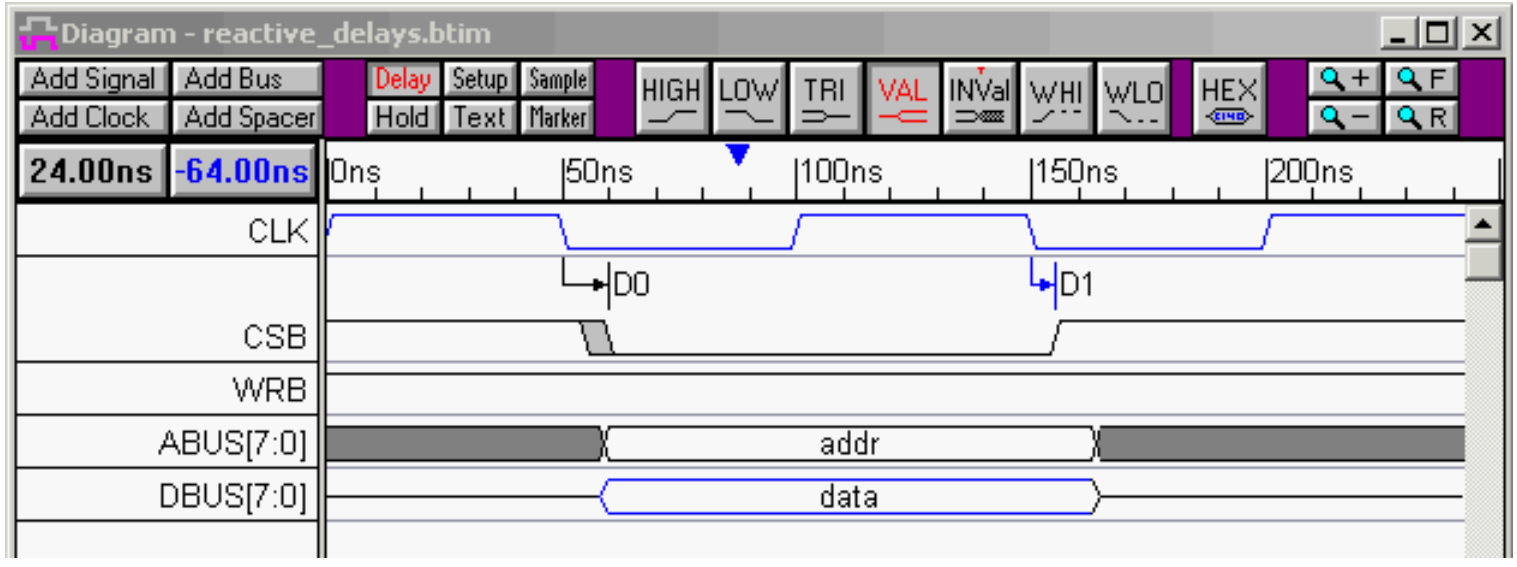
Delays Parameterize Time Values

- Delays represent the time between two edges in the diagram
- Specify min and max values
- Delay values can be time or cycle-based
- Conditionally control when edges occur



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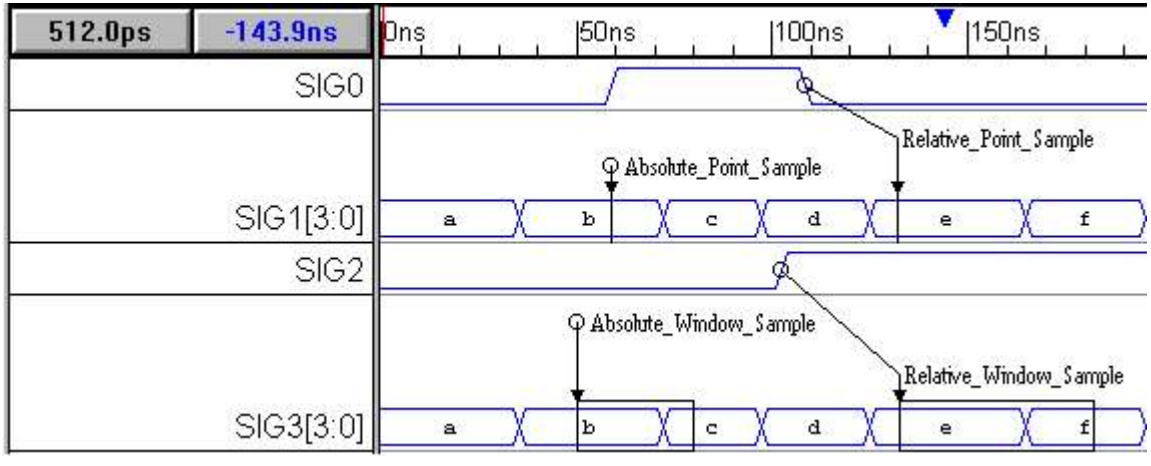
Samples Verify MUT Output

- Sample constructs can monitor and perform actions based on the data sampled
- Sample can work at a single point or over a windowed area
- They can perform relative to the beginning of the transaction or relative to another event in the diagram.



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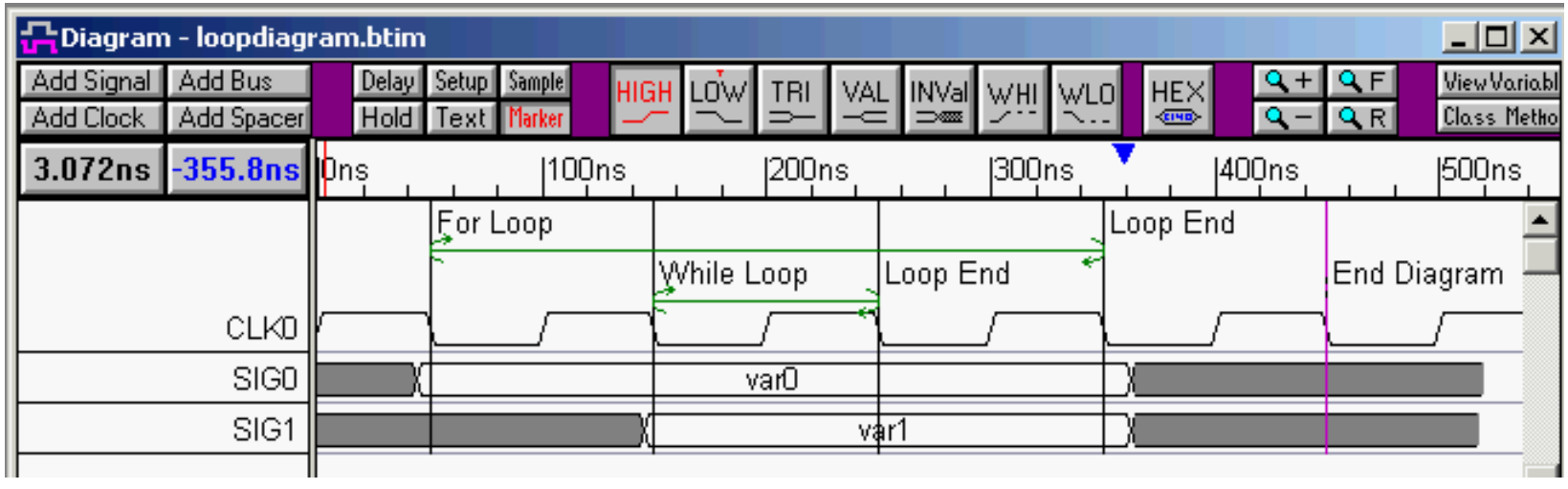
Markers used for Control & Looping Sections of Transactions

- Specify the End of Transaction
- Create loops using *for*, *while*, and *repeat* loop markers
- Insert HDL code



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Reactive Upgrade Options

Features	Non-Reactive	Reactive TB
WaveFormer Pro, VeriLogger Pro, DataSheet Pro	Standard	Optional
Extract signal information from HDL models	Yes	Yes
Generate stimulus models for VHDL and Verilog	Yes	Yes
Draw waveforms	Yes	Yes
Generate waveforms from time-based equations	Yes	Yes
Draw delays, setups, holds, samples, and markers	Yes	Yes
Generate Reactive VHDL and Verilog test bench models		Yes
Samples generate code to verify reaction of MUT during simulation		Yes
Markers create loops to repeat waveform sections		Yes
Variables drive state values in waveforms		Yes
Delays parameterize time values during simulation		Yes
Clock-based test benches		Yes

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