

SynaptiCAD Big Feature List

Timing Diagrammer Pro, WaveFormer Pro, VeriLogger Pro, DataSheet Pro, TestBench Pro, GigaWave Viewer

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SynaptiCAD was founded in 1992 to provide affordable high quality timing diagram editing tools. Since that time we have expanded our product line to include: VHDL & Verilog test bench generation, timing analysis, stimulus generation, Data Book documentation, and Verilog simulation. SynaptiCAD products include:

- **GigaWave Viewer** A waveform viewer and high performance waveform compression engine
- **Timing Diagrammer Pro** A timing diagram editor and timing analysis tool
- **WaveFormer Pro** A waveform translator and RTL simulator
- **DataSheet Pro** A professional datasheet design environment
- **VeriLogger Pro** A Verilog simulator with unit level testing
- **TestBench Pro** a VHDL and Verilog bus-functional model generator

Below is a partial listing of features contained in the SynaptiCAD Product line. The special starred features* are features that we have not seen in other currently available timing analyzer packages. Feature sets change, however, so we recommend that you get an evaluation of our product and try out the features. We think you'll agree that not only are SynaptiCAD's products the best priced timing diagram editors on the market, they are the most powerful and user friendly.

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Waveform Translation Features

The waveform translation features are included in WaveFormer Pro, DataSheet Pro, VeriLogger Pro, and TestBencher Pro products. These capabilities allow the import and export of timing diagrams to other EDA tools, logic analyzers, and pattern generators. For example, you can take waveform output from your simulator or logic analyzer and add timing parameters and textual information to clarify the meaning of the waveforms. You can also graphically generate your digital test vectors in WaveFormer and produce a VHDL, Verilog, or SPICE file that can be read by your simulator. Finally, you can use WaveFormer as a test vector translation tool to port your stimulus vectors from a VHDL/Verilog simulator into a Pattern generator, or from a logic analyzer into a VHDL or Verilog test bench.

*One of the most powerful features of WaveFormer is the built-in scripting language, Waveperl. With Waveperl you can write your own import/export scripts to support any waveform format, including formats for custom software and test equipment. Waveperl can also be used to add custom drawing functions to WaveFormer. Included with WaveFormer are several scripts written by SynaptiCAD. Below is a list of some of the file formats supported by these scripts:

Input Formats

- Standard Formats:

- **Verilog Change Dump (*.vcd)** reads waveforms generated by Verilog Simulators.
 - ***Test Vector Spreadsheet (*.txt)** reads waveforms generated inside spreadsheets.
 - ***Xilinx/Aldec Waves Vectors (*.vec)** reads waveforms generated by simulators that support the VHDL Waves format.

- Test Equipment:
 - ***Agilent Logic Analyzer (*.hpl)** reads data files captured by Agilent and HP Logic Analyzers.
 - ***Agilent Infinium Oscilloscope** can be imported into WaveFormer and used to create VHDL and Verilog test benches.
 - ***Tektronix Logic Analyzer (*.txt)s** reads data files captured by Tektronix Logic Analyzers.
 - ***Podalyzer Data (*.dat)** accepts waveform files captured by Boulder Creek Engineering's PC-based logic analyzer.

- Simulators:
 - ***Accolade VHDL (*.awf)** reads waveforms generated by Accolade Design Automation's PeakVHDL and PeakFPGA simulators.
 - ***Advanced PLD (*.wvf)** reads waveforms generated by Protel Technology's Advanced PLD simulator.
 - ***DesignWorks (*.txt)** accepts waveform files generated by Capilano Computing's DesignWorks' gate-level simulator.
 - **Protel Advanced PLD (*.wmf)** reads waveforms generated by Protel's Advanced PLD simulator.
 - ***SpeedWave (*.vwf)** reads waveforms generated by Viewlogic's SpeedWave VHDL simulator.
 - ***SpeedWave (*.vcd)** reads waveforms generated by Viewlogic's SpeedWave VHDL simulator.
 - ***Workview WFM (*.wfm)** accepts waveform files produced by Viewlogic's Viewsim® simulator.
 - ***Xilinx/Aldec Waves Vectors (*.vec)** accepts VHDL Waves Files generated from any compatible simulator including the Foundation series simulators offered by Aldec and Xilinx.

- Timing Diagram Formats:
 - ***Timing Project (*.tim)** signals and parameters from SynaptiCAD products including Timing Diagrammer Pro, WaveFormer Pro, VeriLogger Pro and TestBench Pro. To ensure file compatibility, open files created with products of the same or earlier version number.

- **TDML (*.tdml, *.tdm)** saves entire timing diagram and timing parameter table in the industry standard on-line data sheet format TDML.
- **Chronology (*.td)** accepts timing diagram files from Chronology's® timing diagram editor.
- **Test Free Parm (*.txt)** is used for editing libraries saved in the standard spreadsheet compatible file format: comma and tab separated text files that contain a header (first line must be "NAME, MIN, MAX, COMMENT").
- **Free Parm (*.fp)** saves just the free parameters in Timing Project File Format. This is one way to make a library file.

Output Formats

- Generic Simulation Formats:
 - ***VHDL transport testbench (*.vhd)** saves the waveforms to a VHDL testbench that uses assignment statements.
 - ***VHDL wait testbench (*.vhd)** saves the waveforms to a VHDL testbench that uses wait statements.
 - ***Verilog (*.v)** saves the waveforms as Verilog stimulus statements.
 - ***SPICE sources (*.cir) and SPICE sources (*.cir)s** saves the waveforms in a format that can be read by all SPICE simulators.
 - ***Pspice(tm) Digital SPICE format.**
 - ***ABEL stimulus (*.abv)s** saves waveforms to an ABEL testbench.
- Standard Simulator Formats:
 - ***Accolade's PeakVHDL and PeakFPGA packages** are VHDL simulators that accept either of the transport or wait state VHDL testbenches. Input also supported.
 - ***ALTERA Vector Format (*.vec)** saves waveforms to a format used by the ALtera Max PlusII simulator.
 - ***Mentor Quicksim II (*.f)** saves the waveforms into a force file that can be read by Mentor's QuickSim II simulator
 - ***Minc PLD-Designer(*.stm)** saves waveforms into a format that can be used by Minc's PLD-Designer Package.
 - ***ModelSim Force File (*.sim)** saves waveforms into a force file that can drive signals in Model Tech's ModelSim simulator.
 - ***OrCAD simulation** is a VHDL simulator and accepts either the transport or wait state VHDL testbenches
 - ***SPICE digital (*.fst)** saves the waveforms into PSPICE digital format.
 - ***VHDL Waves Vector file (*.vec)** Waves stimulus standard for VHDL.
 - **Workview CMD (*.cmd)** saves the waveforms in a format that can be read by Viewlogic's Workview simulator.

- ***Xilinx/Aldec/Orbit (*.asc)** saves the waveforms in the format used by the Xilinx Foundation Design Kit simulator, Aldec, and Orbit's ASIC test vector format.
- Test Equipment Formats:
 - ***HP Pattern Generator (disk) (*.hpd)** exports waveforms compatible with Agilent and HP digital Pattern Generators.
 - ***HP Pattern Generator(bus) (*.hpd)** exports waveforms compatible with Agilent and HP digital pattern generators.
 - ***Tektronix Pattern Generator (*.txt)** exports waveforms compatible with the Tektronix Pattern generator TLA7PG2 and the Tektronix DGLink software.
 - ***STIL Test Vectors (*.stl)s** generates test benches in IEEE Standard P1450 Standard Test Interface Language.

****Waveform Generation Features***

SynaptiCAD's timing diagram editor and simulator tools include the ability to generate signal waveforms from equations. These features augment the drawing environment, and provide a quick way to generate signals without having to draw each signal transition. They also provide a way to generate signals that have precise edge placement.

- ***Temporal Equations** are time-based formulas that concatenate waveform sections to the end of a signal. They provide a quick way to generate signals that have a known pattern that is more complicated than a periodic clock.
- **Boolean Equations** combinatorially relate one signal to other signals in the diagram. This feature greatly reduces the amount of time needed to draw a timing diagram, especially one that models gate level circuits. A special **delay** operator allows modeling of propagation and interconnect delay times. (Not available in Timing Diagrammer Pro).
- ***Spreadsheet-based test vector generation.** Users can create raw test vectors using their favorite spreadsheet software to edit the vectors and then import them to WaveFormer for conversion into VHDL, Verilog, SPICE, and gate simulation formats. Spreadsheet-based test vector generation can be combined with test vectors drawn in WaveFormer's various equation formats, setting a new standard for power and ease-of-use in test vector generation.
- ***State Label Equations.** Automatically generate bus states for counter and shifter type data buses using State Label equations. State Label equations are very useful for creating complex, quasi-repetitive bus signals that are very time consuming to create manually. For example, the following equation would create a bus signal named CNTR that starts

counting from 64 by fours for 100 clock cycles, repeating the entire sequence 4 times: CNTR Rep(Inc(64,4,100),4)

****RTL-Level Simulation Features***

SynaptiCAD supports two different types of simulation environments: RTL-level wizard-based simulation, and standard Verilog simulation. The features in this section refer to the RTL-level simulator included in WaveFormer Pro and DataSheet Pro. These features are also standard in VeriLogger Pro and TestBencher Pro, but are not the primary purpose of these products. With this type of simulation, users can quickly begin to simulate design ideas without having to write a complete HDL model or create a schematic.

- *IEEE 1364 compliant Verilog simulation engine that supports all major constructs of the language, including advanced features such as pin-to-pin timing and PLI interface routines.
- *Registered signals support flip-flops and latches. A point-and-click interface allows selection of edge triggering, level triggering, clocking signal and timing parameter information.
- *Synchronous and Asynchronous Set and Clear. The Logic Wizard now supports registers and latches that have *set*, *clear*, and *clock enable* lines. These feature are particularly useful for designing divide-by-2 circuits and FPGA circuits. Older files that use the start state feature will continue to simulate correctly. The use of a *set* or *clear* line in an older file overrides the obsolete *start state* value.
- 64-Bit math classes allow the simulation of approximately 80s worth of time with 1ps resolution. This means improved performance for users of large data sets captured by HP logic analyzers and simulation runs.
- Global* and individually definable options for timing parameters of registers and latches.
- Simulator supports min timing, max timing and min-max timing for gates, registers and latches.
- One-time and continous* setup, hold and pulse-width time checking.
- Simulation is tightly integrated with built-in static timing analyzer.
- *Simulator supports behavioral constructs be allowing the user to directly enter HDL code.
- *Vector (multi-bit equations!) support includes all normal math operators.
- *Support for tri-state gates and tri-state gating functions.
- *Support for multiplexing functions in equations.
- *Equations syntax supports an extended form of Verilog and VHDL equations that allows easier representation of combinatorial logic (multiple

delays can be embedded into a single expression and min-max timing information is much easier to express). The extended format is converted automatically to standard HDL that can be handled by third party tools.

Ex: Extended Verilog with multiple delays: **sig2 = #5 (#10 sig0) & (#10 sig1)**

Ex: Extended VHDL with min/max timing variables: **sig2 = sig0 and sig1 after Tpd** would perform a min/max simulation of the AND gate using the min and max times specified for Tpd.

- *Ability to turn off continuous simulation mode and to perform one-time simulations on signals that are not continuously simulated.
- *Support for reconvergent fanout analysis in Boolean equations.
- *Signals can be switched back and forth between graphically drawn, and simulated modes.
- *User-definable gate primitives, modules, logic functions and math functions.
- *Support display of simulated vector results (virtual buses) in a variety of formats including binary, hex, and decimal.
- *Report window that allows the display and editing of HDL models generated by WaveFormer Pro, the results of simulation runs, and the execution of Perl scripts.
- Simulation status indicator on button toolbar that displays success/failure information about last interactive simulation. Makes it easy to spot when there is a mistake in your Boolean equations or Verilog code.
- MSB and LSB of multi-bit signals can be set directly in the signal name by bracketing this information (e.g. ADDR[31:0] sets MSB to 31 and LSB to 0). Changing MSB or LSB also changes display of signal name appropriately.
- *Report Window automatically displays vector stimulus and test bench files generated using the Export functions (Export menu options).
- ***Macros** can now be used in waveform segments and Boolean equations. This is a handy way to assign symbolic names to commonly used constant values such as instruction set assignments for microprocessors or constant values such as addresses on a bus.
- *****Waveform comparison** provides comparison between individual signals or entire diagrams.

Signal Features

The Signal features are included in all the products: Timing Diagrammer Pro, WaveFormer Pro, DataSheet Pro, VeriLogger Pro, and TestBencher Pro.

- **Copy/Paste** Signal Waveforms and attached parameters and text.
- **Signals** with 7-state logic: high, low, tristate, valid, invalid, *weak high, and *weak low. *Multistate logic using HEX and binary bus segments. Virtual state information for representing abstract data types in hardware description languages (e.g. support for integers and enumerated data types).
 - *Signal names can have a bar (line) on top to indicate an active low signal.
 - *Left mouse button always draws and edits signals
 - ***Snap to Edge Alignment Grid** allows quick placement of edges which line up with clock edges or other signals.
 - Drag and drop signal edge transitions.
 - Signals can be hidden and moved.
 - ***Block Copy Waveform sections** in the timing diagram (horizontally in time). Possibly the all-time most requested feature. This makes it easy to repeat a section of waveforms (e.g. to create multiple copies of a write cycle on your diagram).
 - Color coded signals indicate direction.
 - Change the level of a segment with only two mouse clicks. Left click on the segment then left click on a state button (High, Low, Tristate, Valid, InValid, Weak High, Weak Low).
 - *Insert Segment into signal by clicking and dragging within a signal.
 - Delete part of a signal by selecting it and typing the delete key.
 - Exact placement of signal transitions with the Edge Placement Dialog box. (Just double click a signal transition and enter a time value).
 - Locked edge option so that a signal transition cannot be dragged or shoved from its current position.
 - Each signal transition can have its own multiple delay reconciliation function (delay reconciliation functions allow the user to specify how multiple delays force a single transition).
- ***Analog Signals** can be created and displayed as analog waveforms or digital buses. Each signal has a complete set of analog properties that control how digital values are converted into analog values. If a signal has a radix of real, the values of the signal will be exported directly as voltage values. If a signal has a radix except real, an internal Digital to Analog converter will use the bus size and the logic voltage level settings to convert the digital waveform value into an analog value
- **Clocks** draw themselves based on their attributes: period of frequency, duty cycle, edge jitter, offset and other parameters. Clocks can also be related to other clocks by creating master clocks or by using formulas that reference another clock's attributes like period, offset and jitter (see [Clocks with Formulas](#)).

- *Clock dialog is fully interactive and updates clock as you change attributes.
 - Insert/Delete clock cycles
 - Edit an existing clock by double left clicking on a clock segment.
 - Exact placement of a clock edge found by double left clicking on the clock edge.
 - Draw Grid from clock edges (specify color, style, and grid spacing).
- **Clocks with formulas** allows modeling circuits that modify the system clock like a "divide by 2" circuit or a clock distribution chip, it is necessary for some clocks to be related to other clocks.
 - Use formulas to specify clock attributes (period, offset, rising and falling edge jitter) in a clock dialog.
 - Reference Clock field in the Clock Properties dialog makes it easier to define sub-clocks (dependent clocks) in terms of reference clocks.
 - *Reference clock parameters in other formulas (i.e. $2 * \text{CLK1.period}$). This allows you to easily determine how timing requirements change as your clock frequency changes.
 - Use extended state information to label clock cycles. The extended state information automatically centers itself within the cycle and adjusts as you change clock frequencies.
- ***Group Buses** are a specialized kind of signal that automates the drawing of timing diagrams. Buses allow the user to edit or draw many signals at the same time. Drawing each signal of a bus is tedious even when using a drawing program. However if the signals are merged into a composite bus signal then only this signal needs to be drawn or edited. Any changes made to the bus signal will be reflected back into the member signals. Bus states can generally be displayed/edited in binary or hexadecimal.
 - *Compress several signals into a bus signal, or create a new bus and its member signals.
 - *Draw all the member signals of a bus at once by using the HEX mode and drawing the bus
 - *Edit all the signals of a bus at once by left clicking on a bus segment then left clicking the HEX button and typing in the new state. (Edits just like signals)
 - *Bus displays hex or binary representation of the signals (Options/Drawing preferences)
 - *Insert a new bus segment by double left clicking on the bus
 - *Hide member signals on Bus merge option
 - *Bind and UnBind member signal transitions inside Buses
 - *Align signals to a bus edge

- **Virtual Buses** are regular signals with virtual state information defined for each segment.
 - Make a signal look like a group bus without the computational overhead of all of the member signals.
 - *VHDL and Verilog stimulus generation supports virtual bus export.
 - *Set virtual bus size by double left click on signal name to open the Signal Properties dialog.
- ***Automatically generate bus states** for counter and shifter type data buses using Auto State Label equations. State Label equations are very useful for creating complex, quasi-repetitive bus signals that are very time consuming to create manually. For example, the following equation would create a bus signal named CNTR that starts counting from 64 by fours for 100 clock cycle, repeating the entire sequence four times: **(CNTR Rep(Inc(64,4,100),4))**.
- ***The built-in functions for Auto State Label equations** enable you to generate most bus sequence types, but it is also very easy to add your own unique functions (written as short Perl routines).
- ***Time Breaks that compress time:** Time breaks are special markers that can compress time, the section of time still exists, but will not display on the screen. Time breaks can be used as an aesthetic graphical display, or as a true time compression marker. There are three graphical time break styles (dotted, curved, and jagged) that emulate the most common time breaks used in data books.
- **Signal Filters:** Control what you see using the filter dialogs to filter signals and parameters - use powerful features within testing and keep your viewing area simple.

Parameter Features (Delay, Setup, Hold, and Sample)

The Parameter features are included in all the products: Timing Diagrammer Pro, WaveFormer Pro, DataSheet Pro, VeriLogger Pro, and TestBencher Pro.

- **Delays:** Force edges to a fixed distance.
- **Setups and Holds:** Monitor time between signal transitions.
- **Samples:** Graphically indicate a point at which a signal should be sampled (e.g. latched or registered). See the TestBencher Pro feature section for specific code generation properties.
- **Using Parameters**

- *Add delays, setups, holds and samples using the right mouse button so you can always draw with your left mouse button.
 - Edit parameters in the diagram window by double clicking on it or edit in the parameter window spreadsheet
 - *Drag and Drop parameter edges to change starting/ending positions of parameters on signals.
 - *Drag transitions from either min or max edge for more control over edge placement.
 - Multiple delays can force a single transition (4 reconciliation methods available).
 - *Min Only and Max Only delays that only affect one edge of a transition
 - Transitions can have overlapping uncertainty regions (option can be turned off).
 - Edit parameters in the diagram window using the Parameter Properties dialog box (Just double click on the parameter).
 - Smart Parameter Sharing
 - *Smart Parameter Lookup in the Parameter Properties dialog box allows you to easily use data from existing parameters by using an existing parameter's name.
 - Move parameters in spreadsheet using drag & drop
 - Adjustable column widths in parameter spreadsheet
 - Hide and delete in parameter window

- Formulas and Operators
 - *Delay, Setup, and Hold timing parameters can be referenced in other parameter formulas (i.e. **D1.max = 2*D0.min**).
 - Free parameters: Parameters not attached to edges that can be used in other parameter formulas.
 - *Different formulas can be given for MIN and MAX parameter values to model complex timing relationships.
 - *Can use .min and .max attributes to access either value of a parameter in any formula. This allows you full control of formula evaluation unlike other timing analyzers which generally force you to accept their interpretation of which value to use. Also prevents the need for non-standard mathematical operators.
 - Parameter label text is completely customizable with control codes (i.e. parameter labels like "tpCK2O [10,20]").
 - "Display time units" setting so that you can enter values at a convenient level and still have the resolution of a smaller "base time unit".
 - *Easy-to-use formula and data entry that doesn't require annoying brackets and commas.

- Display of Parameters

- ***Realistic Data Book Parameter Names** like t_{pd} supported with subscript, superscript, bold, and italic formatting.
 - Control codes can also be placed in text strings so that you can put edge times in your text that automatically update.
 - Drag & drop parameters to a new vertical position, including positions between a new pair of signals.
 - Selectively display all objects of a given type: delays, setups, holds, and text
 - Toggle switch for color coding of delays for perfect black and white printing (View\Show Critical Paths...).
- **Parameter Filters:** Control what you see using the filter dialogs to filter signals and parameters - use powerful features within testing to keep your viewing area simple.

Advanced Timing Analysis Features

The advanced Timing Analysis features are included in all the products: Timing Diagrammer Pro, WaveFormer Pro, DataSheet Pro, VeriLogger Pro, and TestBencher Pro.

- *****Delay Correlation:** SynaptiCAD's timing diagram editors have the capability of specifying a correlation percentage between timing delays. This lets you account for the correlation in delay times between gates on a single chip. For example, the absolute delay for gates on a FPGA might be specified in a datasheet as 5-10ns (min/max). This min/max delay variation is due to variations in the particular batch lot of the chips and potential variations in operating temperature. However, the maximum delay difference between any of the gates on a given chip is much smaller than the worst case given in the datasheet (all the gates came from the same lot since they are on the same chip and they are operating close to each other in temperature). To model this in WaveFormer, you can specify the min/max delay from the datasheet and a correlation percentage that indicates how much variation there can be between the correlated delays (100% correlation meaning that the delays on all the gates will happen at exactly the same time and 0% meaning the delay times are randomly distributed as if they were gates on different chips).
- **Reconvergent Fanout:** Automatically removes common signal delay uncertainties from setup and hold margin and distance calculations.
- **Multiple Delays** on a single transition:
 - Four methods of reconciling multiple delays: earliest transition, latest transition, min uncertainty, max uncertainty.
 - *Ability to set the default reconciliation method for multiple delays.

- ***Visual display of min/max critical paths** using color coded delays to indicate which delays are forcing the min and max edges of a transition. This type of critical path display is necessary in diagrams where multiple delays drive a signal transition. The colors are: Gray = none, Blue = Min only, Green = Max only, Black = both min and max.
- ***Ability to specify minimum uncertainty on a transition** (from Edge Placement dialog). If no delays cause an uncertainty greater than the transition's minimum uncertainty, the transition will be given its minimum uncertainty value.
- ***Min Only and Max Only Delays:** delays that only affect one side of a transition.
- *Delays turn red when violated: Especially useful for determining dominant delays when multiple delays are forcing an edge.
- Setups and holds turn red when their margins are violated.
- Parameter Sharing: sharing of parameter values by several parameters.
 - Smart sharing automates sharing of parameters for same edge types between two signals.
 - *Share by name change. Makes it easy to share and unshare parameter values (this can be very tedious in other packages).

Measurement Features

The Measurement Features are included in all the products: Timing Diagrammer Pro, WaveFormer Pro, DataSheet Pro, VeriLogger Pro, and TestBencher Pro.

- ***Modeless Measurement:** Measurement is an integral function of timing analysis and with WaveFormer, relative and absolute measurements are always displayed on the screen. There is no special measurement mode that you have to get into and out of and no clunky cursors to drag around.
- ***Relative Measurements (distance between two objects):** Get the relative time between two objects with only two mouse clicks. Left click on the first object. This moves the blue delta mark to that position. Now the blue readout/button above the signal names will display the distance between the blue delta mark and the mouse cursor. If the left mouse button is pressed down on an object like a signal transition then that object can be dragged while the delta display shows the relative time between the objects.
- **Absolute Measurement with the mouse:** The time display always shows the position of the mouse in the diagram window. To find the location of an object in the diagram window, place the mouse on top of the object and read the time display.

- **Exact Absolute Measurement of an Edge:** Double clicking on a signal transition will cause the "Edge Properties" dialog box to display the min and max time of the transition.
- **Display the position or uncertainty of an edge:** Get into the Text mode. Left click on an edge, right click to open an edit box. Enter %m, %M, or %u control codes to display min transition, max transition, or uncertainty region.
- **Display the distance between two transitions:** Add a delay, setup, or hold parameter between the two transitions. Double click on the parameter to open the "Parameter Properties" dialog box, and choose distance radio button.
- **Time Markers display an exact time:** Add time marker by left clicking on the Marker button and then right clicking in the diagram window. Edit a time marker by double left clicking on the time marker line. The End time marker indicates where to stop generating stimulus.

Usability Features

The Usability Features are included in all the products: Timing Diagrammer Pro, WaveFormer Pro, DataSheet Pro, VeriLogger Pro, and TestBencher Pro.

- **Multiple Undo and Redo:** Undo up to 20 previous drawing and editing actions. The **Undo Delete** menu option remains, so deletes can be undone without changing the multiple undo/redo buffer.
- ***Modeless Drawing:** Ever wonder why some CAD programs are mode intensive? To perform even the simplest editing and drawing you have to be in the correct mode. WaveFormer allows you to draw and edit waveforms no matter what mode you happen to be in.
- ***Modeless Edit Bus State Dialog**
- ***Group Edge Shifting** allows moving all edges in a signal. Hold down the or key while dragging a transition causes all the transitions to the right or left of the selected transition to also be moved. Holding down both keys causes all the edges in the signal to also move.
- ***Centered Zooming** about a selected edge and regular zooming from the center of a diagram.
- ***Object Oriented Drawing Environment:** WaveFormer is an object-based drawing environment. This means you will be able to extrapolate most functions if you know how to do something similar. For instance, one way to delete a signal is to select it by left clicking on the signal name then pressing the delete key on the keyboard. Similarly, to delete a delay object, select it with the left mouse button and press the delete key.

- ***Optimized code(fast drawing, scrolling, file loading, and program loading):** After WaveFormer was written, designed and debugged we went back and made it better. Many Windows(tm) programs are slow, but we took the time to make ours fast. This was especially critical to support the file translation capabilities of WaveFormer as it has to be able to handle diagrams with hundreds of signals and several hundred thousand signal transitions.
- ***Drag & Drop File Load:** From File Manager or Explorer you can drag a .tim file (WaveFormer's normal output file) and drop it onto a diagram or parameter window to open the file. This is helpful if you have a lot of timing diagrams and would like to view them in rapid succession (You can also double click on the first one to start WaveFormer).
- **File History List:** The File menu has a history list of the last four files that were used. This helps you quickly load your current project. Left click on a file in the history list to open that diagram (or use ALT-F1 to open the last file you worked on).
- **Intelligent Windows:** The Diagram and Parameter windows remember their size and location the last time the program was run. This means that you don't have to size and move the windows each time you run the program. Fonts, colors, and window specific options are also remembered.
- **Proportional Scroll Bars:** The thumbs on the scroll bar are proportionally sized to indicate how much of the window is being viewed.
- ***Pushed in Buttons:** WaveFormer's buttons looked pushed in when they are activated. No squinting necessary to detect that dotted gray box around a normal Windows' button.
- ***Space Efficient Status bar and Quick Overviews:** Nobody wants to read the entire help before they use a program for the first time so we have status bars and two short overviews to help new users get started. Our status bar is displayed on the window title bar to save on screen real estate.
- ***Convenient Naming** of Buses, Signals, Clocks, & parameters (Right click on add or mode button to change the default naming prefix). This makes it easy to create several objects with iterating names (i.e. tp1, tp2, tp3, etc.).
- ***Turn on/off State Button toggling.** Double click on a state button to turn off toggling. Click on another state button to turn toggling on again. Makes it easy to draw signals consisting of a number of valid segments.
- ***Edit Box History Lists:** Many edit boxes are equipped with permanent history lists that store information from session to session. History lists save the user from retyping previously entered information. History lists are stored in the timing.ini file in the Windows directory and can be pruned

and rearranged in that file (be sure WaveFormer is not running while editing this file or changes will be lost when WaveFormer is closed).

- ***Compact dialog boxes** allow maximum use of your screen real estate (great for laptops).
- ***Context sensitive help** for dialogs provides immediate reference for features and links directly to online help
- **Lock or unlock all the edges** on user-selected signals by choosing menu option Edit > (Un)Lock Edges of Selected Signals.
- **Reactive Cursor Indicates Editing Operations:** The cursor changes shape to indicate the different editing options available for particular objects.

object	cursor	action
parameter	up-down arrow	move parameter up or down
parameter handle	pointer	drag handle to new edge
text	four-way arrow	drag or nudge in any direction
marker or edge	left-right arrow	drag or nudge left or right
all other objects	cross hair	regular editing and drawing

Library Features

The advanced Library features are included in all the products: Timing Diagrammer Pro, WaveFormer Pro, DataSheet Pro, VeriLogger Pro, and TestBencher Pro.

- Ability to browse part libraries and insert parts directly into project.
- Reference parts without including them in the project so that when the libraries change your diagrams are automatically updated.
- ***Copy referenced parameters into your project to make it self contained.** This makes them easy to move and freezes them so that future library changes will not disturb your project.
- Update project from libraries so that self-contained projects can be updated if necessary.
- ***Easy part referencing.** Insert library parameter names directly into formulas by pressing the library button or F3 key and selecting parameter from library parts dialog. Parameter names are placed at current cursor location.
- ***Faster Library Specifiers:** The Edit Macro dialog finds the library specifiers that are defined for the current project and displays them in the

Value drop down list box. This simplifies and speeds up the process of switching between libraries.

- Hide parameters in parameter spreadsheet window.
- Able to import & export library parameters to spreadsheets in tab separated value format.
- Able to read Chronology(R) libraries.
- *Easily create custom libraries by saving free parameters from any project.
- Macros enable you to make short names for parts and quickly switch vendor libraries and parts.
- Library files can be placed in different directories and even on different machines so networked users can share a common set of library files.

Documentation Features

These documentation features are included in all the products: Timing Diagrammer Pro, WaveFormer Pro, DataSheet Pro, VeriLogger Pro, and TestBencher Pro.

- Realistic Data Book Display Features
 - * **Realistic Data Book Parameter Names** like t_{pd} supported with subscript, superscript, bold, and italic formatting.
 - *All text objects and parameter comments support subscript, superscript, bold, and italic formatting.
 - *Signal names with an over bar (line on top) indicate active low signals.
 - *Edge placement grid makes it easy to line edges up with clocks or other signals edges.
 - *Text placement grid makes it easy to align multiple lines of text.
 - *Scaleable **FrameMaker MIF** images. Once our MIF images are imported into FrameMaker you can grab the edge of the image and scale the image as desired.
 - *Ability to set horizontal size of **FrameMaker MIF** images. Useful when generating multiple MIF images of the same size.
 - *Group Edge Shifting allows moving all edges in a signal for quick editing of the timing diagram. Use CTRL and SHIFT keys individually or in combination while dragging and dropping the selected edge.
 - Signal ends can be snapped to a marker. This makes it easy to end all signals at a common time.
 - *Data sheet quality 0-1ns setups and holds. Data sheets often contain many 0ns setups and holds. WaveFormer Pro represents

small setups and holds as two horizontal arrows pointing to a center line for a more professional display.

- Parameter Display Features
 - Drag & Drop control over parameter location in your timing diagram.
 - Control which attribute a parameter will display like: name, min/max time, min/max formula, margin, distance, or comment. Both global and individual object control.
 - *Realistic data book parameter names like t_{pd} supported with subscript, superscript, bold, and italic formatting.
 - *Custom Parameter display: if the normal parameter output is not exactly what you want then design your own custom string. Use control codes to reference a parameter's values inside the custom string. For example: **D0's delay time = %m,%M** custom string would replace %m with the min time and %M with the max time of delay D0. The rest of the string would display as typed. Control codes are available for all parameter attributes. Both global and individual object control.

- Signal Display Features
 - Grid lines can be placed on clock edges in a variety of different styles.
 - *"Smart" Print Settings. The default range for printing the timing diagram window is the **End Diagram Marker**. If there is no End Diagram Marker, then the timing diagram window is printed to the farthest non-repetitive signal edge.
 - *Signal Names can be displayed with an over bar or line on top for active low signals.
 - Control the width of signal name window by dragging & dropping the bar separating the signal names and signal waveforms (nice for printing and image creation).
 - Signals can be displayed with either sloped or straight edges
 - *Control pixel slant of sloped edges
 - *Control waveform line thickness
 - *Control waveform color
 - *Spacer signals improve document appearance (great for titles at top of diagram). Spacers allow you to add extra space between signal names without having excess signal separator lines drawn.
 - *Control codes can also be placed in text strings so that you can put edge times in your text that automatically update.
 - Signal ends can be snapped to a marker so that all the signals in a diagram can easily be made to end at the same time.
 - Right justify signal names using the Drawing Preferences dialog.

- ***Font and color control** (Program Global, Window Global, and Individual Object control). Some programs have limited control, however WaveFormer has it all.
 - *Control of global default font that is used by all windows unless individually specified. This also makes it easy to change the font of all your text objects at once.
 - *Control the font used by individual windows: button-bar, header, diagram, label, and parameter windows.
 - Control the font used by individual text objects.
 - Control color used by signals

- **Support for TDML:** Over the next two years, on-line data sheets are going to augment or supplant printed data books. TDML (timing diagram markup language) is the timing diagram and timing parameter format recommended by the Si2 ECIX committee involved with defining the data sheet standard. With TDML, you will be able to view on-line data sheets (supplied by semiconductor manufacturers) in a browser-like environment, then automatically launch WaveFormer Pro to display and manipulate the timing information. SynaptiCAD has been working with Si2 since November of 1996 to define the TDML standard. We expect to see the first on-line data sheet sites in early 1999. Keep checking our web site for updates on the latest TDML information.

- **Text annotation:** Add comments and titles anywhere in your timing diagrams.
 - *Text placement grid makes it easy to align multiple lines of text.
 - *Text object keyboard "nudging": Use the arrow keys to move a selected text object one grid square in any direction.
 - Multi-line text. Paragraph text blocks can be added by editing an existing text object. The normal Windows copy and paste keyboard shortcuts (CTRL-C, CTRL-V) can be used to copy text to or from a word processor.
 - Text objects can be placed at a fixed time or grouped to a signal transition.
 - Text can be centered inside a signal, bus, or clock segment (especially useful for documenting multiple clocks of a bus cycle or multi-phase clock systems)
 - Individual font and font color control for each text object.
 - *All text objects support subscript, superscript, bold, and italic formatting (CTRL-D, CTRL-U, CTRL-B, and CTRL-I).
 - Drag & Drop to move text.
 - Double left click to edit text.
 - Use right mouse button in text mode to add text.

Image Export & Printing Features

- Copy waveforms to clipboard (bitmap format used by virtually all Windows programs).
- Copy timing parameters to clipboard.
- *Copy to clipboard is WYSIWYG.
- Printing: Horizontal and vertical scaling of your entire diagram. Allows you to fit your diagram on a single page even if you have a large number of signals. Also allows you to scale your entire diagram including fonts.
- Control of header and footer text.
- Control of printer margins.
- Scaled to page printing allows you to autoscale waveforms to fit on a given number of pages.
- Export timing parameters to all major commercial spreadsheets.
- *Five vector image formats for creating publication quality documentation.
 - MIF files for FrameMaker (editable from inside FrameMaker)
 - *EPS files and support for imbedding image previews (good cross-platform format)
 - *CGM metafiles (editable images for Microsoft Office)
 - *EMF enhanced metafiles
 - WMF metafiles (these are written to a file and also put on the clipboard so you can use the Edit\Paste command to insert image into MS Word)

DataSheet Pro Documentation Features

DataSheet Pro provides a standardized exchange mechanism for designers and technical documentation specialists. This solves many of the most serious problems associated with creating IC data sheets by eliminating the need to reenter data, avoiding misinterpretation of specifications, and keeping technical data synchronized between engineers and the published documentation. Besides importing timing diagrams from engineering design tools, DataSheet Pro can also create timing diagrams using its professional editing environment.

- *Built-in timing diagram editor with multiple timing diagram display
- ***Project Management** allows multiple timing diagrams to be listed in the project window, providing easy access to all the diagrams in a particular design. Double clicking on a file name opens the timing diagram for editing.

- ***Style Sheets** make it easy to ensure that a set of timing diagrams conforms to a departmental standard without enforcing the style on the diagram creators.
- ***Multiple Views** let the user to store the settings for multiple pictures (images) taken from a single timing diagram.
- ***Web Compatible and Vector based Image Creation.** Datasheet Pro supports additional formats like PNG, TIFF and JPEG that give documentation specialists the ability to create images for professional environments.
- *****OLE Editing, Object Linking and Embedding,** lets users embed timing diagrams into other publishing programs like Word and FrameMaker. Double clicking on an embedded image launches DataSheet Pro with the selected timing diagram. OLE is also available as an extra feature that can be added onto Timing Diagrammer, WaveFormer, VeriLogger, and TestBencher products.

VeriLogger Pro Simulation

VeriLogger Pro is a low-cost, full-featured Verilog simulator. SynaptiCAD combined many of the best ideas from modern programming IDEs and SynaptiCAD's timing diagram editing environment to create an interactive simulator with graphical stimulus generation.

- ***IEEE 1364 compliant Verilog simulation engine** that supports all major constructs of the language including advanced features such as pin-to-pin timing and PLI interface routines.
- ***Hierarchical browser** that displays the structural relationships of design modules.
- ***Waveform Viewer** for displaying both simulation results and graphical test benches.
- ***Single step debugging** integrated with the editing environment.
- ***Point-and-click breakpoints**
- ***Graphical and console execution simulation engines**
- *****Unit-Level Test Bench Generation.** If your top-level module has ports, VeriLogger automatically wraps a test bench around the top-level module and creates signals in that test bench to drive and watch the top-level module.

TestBencher Pro Features

TestBencher Pro generates VHDL and Verilog bus-functional models from graphical timing diagrams.

- Uses bus-functional model representation
- Generates native VHDL & Verilog code
- Compatible with all major HDL simulators
- *Resulting code is small and easy to debug
- *Supports both time and cycle-based test benches
- *Supports State and Timing parameter variables
- Set parameters at runtime with function calls
- *Set parameters from data files for regression testing
- *Express runtime-computable timing relationships between signal transitions
- *Built-in timing diagram editor with multiple timing diagram display
- *Simple, orthogonal set of graphical constructs to express transaction protocols:
 - ***Drawn Waveforms:** stimulus and expected response
 - ***State Variables:** parameterize state values
 - ***Delays:** parameterize time delays
 - ***Samples:** verify and react to output from MUT
 - ***Markers:** model looping constructs, insert native HDL subroutine calls, or end transaction
- *Methods provided for waveform generation:
 - Graphically draw stimulus/response waveforms
 - *Generate waveforms using RTL-level equations
 - *Import from simulators: VHDL, Verilog, SPICE
 - *Import from logic analyzers: Agilent, Tektronix
 - *Import state information from spreadsheets
- *Parameterize state values using:
 - Function parameters
 - *File variables
 - *Conditionally control edges using delays. Delays can be time or cycle-based.

- Response Checking with Sample parameters. Sample constructs can monitor and perform actions based on the data sampled.
 - *Two basic versions of samples: Single-Point samples and Windowed samples
 - *Each of these samples can either perform relative to the beginning of the transaction or relative to another event in the diagram.
 - Samples conceptually model IF-THEN-ELSE code.
 - Default actions are provided which perform basic logging and error detection
 - *Actions can be added to the interface using native language code segments
 - *Samples can conditionally monitor a sequence of events
 - ***Sample actions can trigger delayed state transitions and other samples. These triggered events can be chained.

- Markers used for control and looping sections of transactions
 - Specify the End of Transaction
 - *Create loops
 - *Insert HDL code
 - ***Useful for generating conditional burst type transactions

- *File associations allow simulation data to be read from and written to files
 - *Input state values
 - *Output sampled state values
 - *Input data from a file that can be accessed randomly for use during simulation

- ***Transaction Manager** that can take lists of transactions from files, transactions applied by other interface models, and randomly generated transaction and apply them to the model under test.

- **External Simulator Control:** TestBencher Pro can control external simulators through it's graphical interface, so that compilation and simulation of the project can be handled without having to exit TestBencher. This is particularly useful when multiple tools are needed to compile and simulate a project. For example, if you are using one of the new verification languages you will need a tool to compile the test bench into either a dynamically linked library or byte code. You will also need a VHDL or Verilog simulator and a make file containing all of the information about your model under test and the commands to dynamically link to the test bench library. With TestBencher, all of these details are automatically handled for you. TestBencher stores information about both your simulator and verification compiler and can remotely call those programs and display the results of the simulation. Supports the following simulators:

- Aldec Active_HDL
- Cadence NC Verilog, NC VHDL, & Verilog XL
- GNU gcc
- Microsoft C++ Compiler
- Model Sim GUI & Command Line
- SynaptiCAD's VeriLogger Pro
- Synopsys VCS & Scirocco
- Synopsys VERA
- Verity Specman Elite

GigaWave Viewer Features

Gigawave Viewer combines SynaptiCAD's WaveViewer with our high-performance gigawave compression engine to create the lowest cost waveform viewer capable of handling multi-gigabyte VCD files. Gigawave viewer also comes with a PLI-based library (coming soon) that can be integrated with your favorite simulator to generate highly compressed BTIM files. Using BTIM waveform dumping can speed up simulation by up to 3x over dumping using an ordinary VCD dump and the resulting files are generally 100x smaller. BTIM files also load much faster than VCD files (typically around 500x faster)! GigaWave also loads SPICE results, TDML, logic analyzer data, and more.

- View multi-gigabyte VCD files
- Generate compressed binary files for fast viewing
- Gigawave Viewer comes with the Gigawave Option installed
- Batch Mode Operation

Multiple Timing Diagram Option

Multiple Timing Diagram Window option enables the user to open and edit multiple timing diagrams simultaneously. This feature is extremely useful for visually comparing different timing diagrams. View one timing diagram while drawing a similar timing diagram in the design. Also view timing diagrams and simulation results at the same time. This feature comes standard with TestBencher Pro and DataSheet Pro and is an optional feature for our other software products.

OLE Option

SynaptiCAD's OLE option puts documentation professionals on the cutting edge by allowing timing diagrams in TIM or TDML format to be included directly into data sheets. OLE (Object Linking and Embedding) provides a quick way to manage image files and the corresponding timing diagram files inside word processing documents. With OLE, word processing programs can embed timing

diagram images which remember the timing diagram file and program which created them. If you double click on the embedded image, DataSheet Pro will automatically launch and load the corresponding timing diagram file. Any changes to the timing diagram file will automatically update the embedded image. This makes it very easy to manage a large number of timing diagrams because two separate files need not be maintained for each diagram. OLE is supported by many of the most popular documentation programs like MS Word and FrameMaker. The OLE option is included with DataSheet Pro, and it can be added to the other SynaptiCAD products.

GigaWave Option

GigaWave File support option allows SynaptiCAD's products to view and edit very large simulation and logic analyzer waveform files. The ability to edit and annotate large waveform files is a unique feature of the SynaptiCAD product line that is not offered by any other product on the market. The GigaWave options uses several advanced waveform compression algorithms and a high-speed, binary waveform database that lets the program load, edit, and compare files that are 200 times bigger than can normally be handled on a given system.

Modern simulation test benches will often generate very large waveform result files, which need to be compared against previous simulation runs or against a reference simulation (for example, comparing gate level simulation results to a RTL or behavioral level model). A similar need to load and compare large waveform sets arises when capturing waveform results from a hardware system with a logic analyzer. With the GigaWave option, you can easily handle these files and perform detailed comparisons between the waveform files, reporting any discrepancies. The GigaWave file support option is a "must-have" feature for engineers who need to view, edit, or compare large sets of waveform data. GigaWave is included in GigaWave Viewer and in the G-Series products. It can be added to the other SynaptiCAD products.

WaveFormer Comparison Option

Waveform comparisons graphically display the differences between compared waveforms for two timing diagrams or individual signals. This feature is exceptionally useful when comparing two different simulation runs, as well as for comparing logic analyzer data to a simulation run. A range of tolerance can be provided using the compare signal settings.

Software Support

We offer free telephone and email technical support to our customers. All members of our technical support staff are experienced digital engineers and are very familiar with the product's operation. Bug reports are our highest priority, and we deliver bug fixes as quickly as possible.

Platform Support

We currently offer native binary support for the following operating systems:

- Windows 95, 98, NT, 2000 and ME
- SunOS, Solaris and HP-UX

Upgrade Path

Because SynaptiCAD's products are written from the ground up in C++ we are able to add new features much more rapidly than most software companies. So please call us for a feature request. (Many of our best features are a direct response to customer requests).

Note: Timing Diagrammer Pro, WaveFormer Pro, DataSheet Pro, VeriLogger Pro, TestBencher Pro, and SynaptiCAD are trademarks of SynaptiCAD Inc. All other trademarks are property of their respective companies.