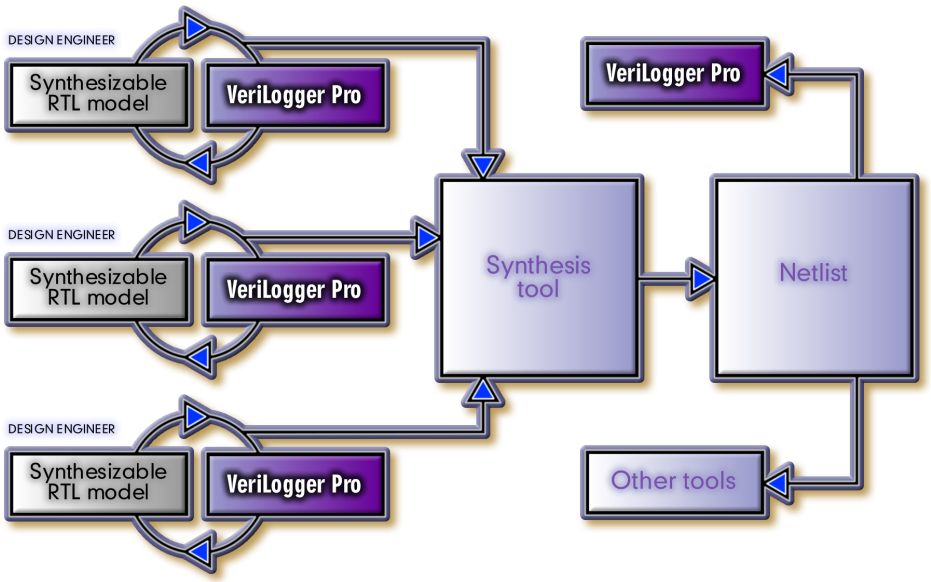
VeriLogger Pro

VeriLogger Pro, by SynaptiCAD, is a complete design and verification environment for ASIC and FPGA designers. It contains a new type of Verilog simulation environment that combines all the features of a traditional Verilog simulator with the most powerful graphical test vector generator on the planet. Model testing is so fast in VeriLogger Pro that you can perform true bottom-up testing of every model in your design, a critical step often skipped in the race to market. Test vectors can be imported or exported from logic analyzers, pattern generators, and 3rd party VHDL, Verilog, and SPICE simulators for reuse. Simulation features include waveform viewing, optimized gate-level simulation, single-step debugging, point-and-click breakpoints, hierarchical browser for project management, and batch execution.

Complete ASIC and FPGA design Environment



In a typical design of a large ASIC, each contributing engineer can use a VeriLogger to develop and simulate their portion of the chip. After each portion has been synthesized and checked, the entire integrated design can be rapidly simulated and verified using VeriLogger with its optimized gate level simulation engine activated. VeriLogger interfaces to synthesis tools, place-and-route tools, and all vendor Verilog libraries. VeriLogger supports design flows using Actel, Altera, Lattice, Lucent, Quicklogic, Vantis , and Xilinx devices with full timing verification using SDF back-annotated simulation models.

Graphical Test Bench Generation

VeriLogger can automatically generate test bench code for your design models. Using the built-in timing diagram editor, just draw the stimulus waveforms and VeriLogger will write the test bench and simulate it with your design models. VeriLogger also includes an instant-feedback simulation mode in which any change to the design code or the waveform stimulus vectors results in an automatic re-simulation. This mode is especially useful for quickly verifying the functionality of small design blocks, making it possible to perform true unit-level testing of designs.

Cut Design Costs By A Factor of 10

If you've wanted to move up to the latest design methodologies, but have hesitated because of the high entry costs, VeriLogger is your answer. If you've already moved to Verilog, but haven't been able to afford to equip all the members of your team with their own simulators, VeriLogger is your answer too. VeriLogger is 100% compatible with Verilog-XL and integrates seamlessly into an XL environment.

Simulation Button Bar

The simulation and debugging functions in VeriLogger are accessed from the simulation button bar located at the top of the main window. One of the unique features of VeriLogger is that it has two simulation modes: Auto Run and Debug Run. The active simulation mode is displayed on the left most button on the simulation button bar. In Debug Run mode, simulations are started only when the user presses the Run or Single Step buttons (similar to a standard Verilog simulator). In Auto Run mode the simulator will automatically run a simulation each time a waveform is drawn or changed in the Diagram window. This mode makes it easy to quickly test small modules and do bottom-up testing.

Stop Simulation

Single Step

Start Simulation

Debug or Auto Run

Waveform Viewing Environment

VeriLogger's diagram window is used to display simulation results and to provide a drawing environment for the graphical test bench generation.

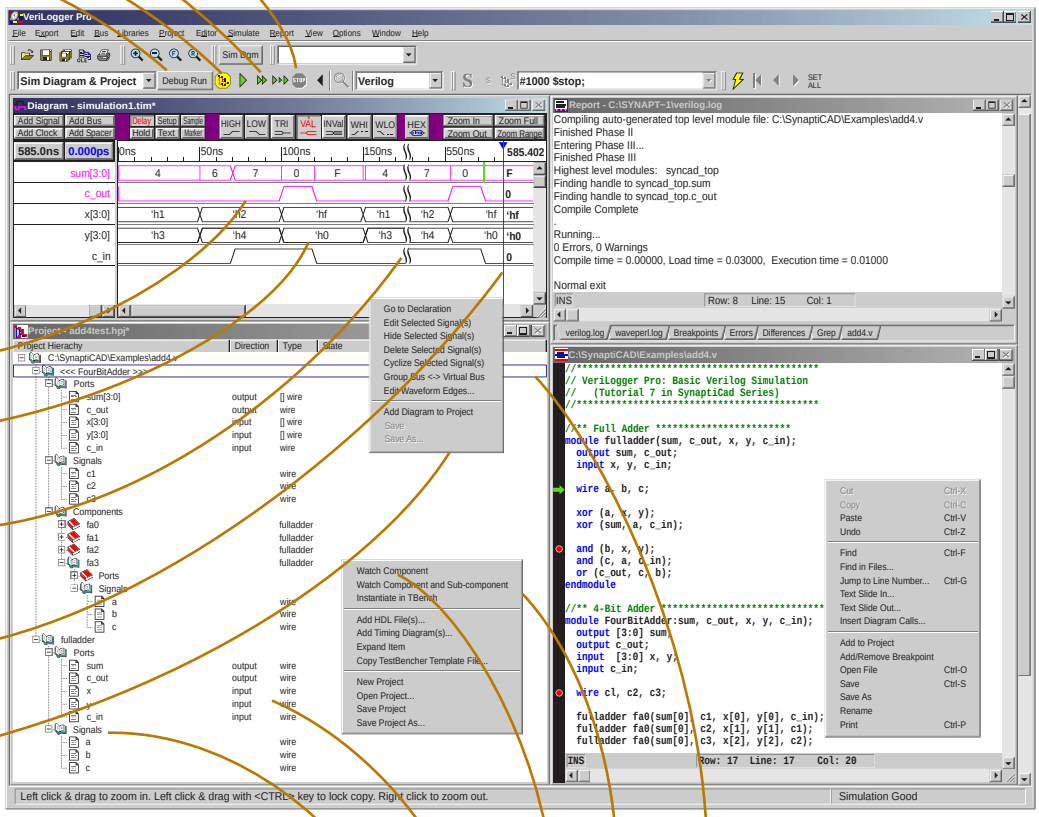
Purple signals are simulation results

Black signals are stimulus that drives the simulation

Markers can be used to hide sections of simulation for easier documentation

Click in timeline to display all waveform values at a particular time

Go to Signal declaration in an editor window



Project Window

The Project Window is used to investigate the hierarchical structure of the Verilog components, navigate source code, and set watches on signals. Each node in the tree has a context-sensitive pop-up menu that can be opened by right clicking on the node.

Show hierarchical structure of Verilog components

View signal direction, type, state

Set watches on ports, components, and signals

Context sensitive pop-up menus

Top-level component in project shown with triple brackets

Comparison Button Bar

Graphically display the differences between compared waveforms for two timing diagrams or any set of signals. This feature is exceptionally useful when comparing two different simulation runs, as well as for comparing logic analyzer waveforms to a simulation run. Supports edge tolerance settings and clocked comparisons.

Compare Signals

Move to next difference

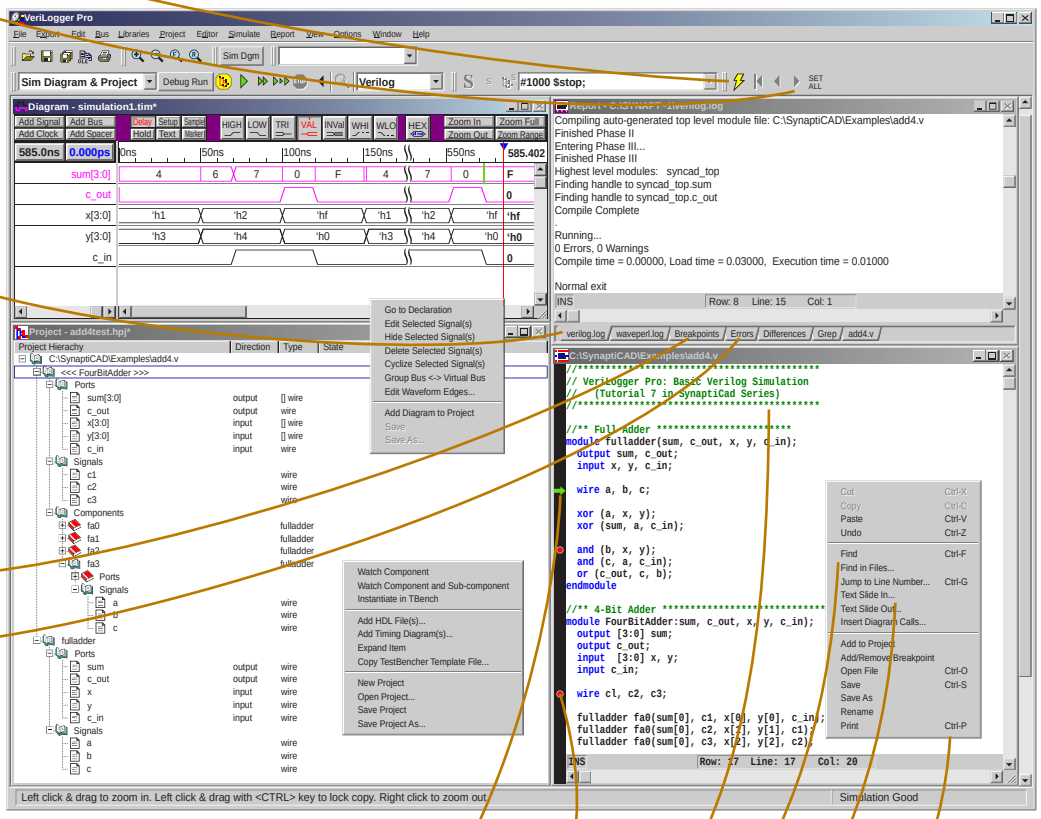
Report Window

The Report window manages several tab windows which are important to simulation and debugging.

Simulation log file contains all information generated by the simulator, such as compiler messages, and all user-generated messages from $display tasks and traces are sent to this file.

Lists the breakpoints in the current project

Hyper-linked list of simulation errors



Editor Window

VeriLogger's editor windows are an integrated part of the simulation environment. Double clicking in the Project Tree, Errors, or Breakpoints windows will open an editor and display the relevant source code. The editor windows are also used to display the current execution line for single-step debugging.

Display current execution line during debugging

Point and Click Break Points

Color-syntax editing

Search and Find in Files

Block Text Features

Context Sensitive Pop-up Menu

Design Flow Intergration

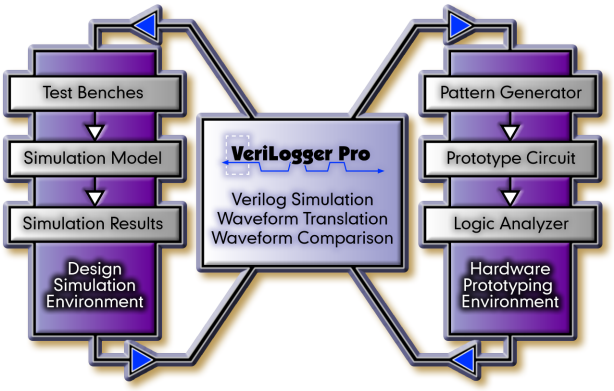
VeriLogger smoothly integrates into existing Verilog design flows. It also supports customization features like a dynamic PLI interface for intergration with 3rd party tools and C / C++ based simulation models The package includes a bundled command-line simulator for batch execution enviroments. The command-line simulator supports de facto standard command line options and debug commands, so there's no relearning for experienced Verilog-XL users. And it includes a built-in Perl interpreter for writing scripts to automate common tasks in your design flow. With the built-in interpreter, you can even execute Perl scripts directly from your simulation code!

Integrating Hardware and Simulation Test Bench Development

VeriLogger Pro acts as a two way translator between simulation and hardware environments, providing you with an integrated platform for test vector creation, analysis of results, and detection of elusive timing problems. VeriLogger Pro reduces verification time for both simulation models and hardware prototypes by taking advantage of the strengths offered by each environment.

VeriLogger verifies Hardware Prototypes

VeriLogger enables you to leverage the work done during the design phase of your system to simplify the development of a hardware test environment. VeriLogger can take waveforms generated during simulation of Verilog test benches to create pattern generator stimulus files, drastically reducing the time to create a prototyping environment. VeriLogger Pro can also verify proper operation of hardware by comparing logic analyzer data to simulation results. Automated comparison guarantees a rigorous check of each data point, ensuring the detection of "small impact" errors that are easily missed during visual inspection of the waveforms. Another benefit of combining a simulation environment with a hardware prototyping setup is the ability to generate timing analysis reports, to detect subtle setup and hold timing violations in the hardware prototype.



Hardware used to Create Verilog Test Benches

Just as design data can be transferred into the test domain to help verify hardware, the reverse process can be applied to the design and simulation of new systems. Most designs need to interface with existing hardware, but simulation models are frequently not available for that hardware. Waveforms from the existing hardware can be captured with a logic analyzer and converted to HDL test bench code or SPICE stimulus and used to test the new system. Instead of spending weeks developing a test bench, you can capture real world stimulus and begin testing within minutes of capturing the data. Existing hardware can also be used to verify that a next-generation system's interface is compatible with the older hardware.

" I'm impressed with SynaptiCAD, they have a great simulator at a very accessible price. I found it to be 100% Cadence Verilog-XL compatible. My test case simulated the same RTL code from a big FPGA (Xilinx Virtex-300/600/1000 and an Altera 10k150) in Verilog XL and in VeriLogger with no problems. Even on a machine with only 128M of RAM, VeriLogger performed well. The SynaptiCAD staff was very quick to answer any questions and I have always found them to be very responsive and helpful. "

Gill Romero
Principal Consultant, ASIC Alliance Corp.

VeriLogger Pro
TestBencher Pro
DataSheet Pro
WaveFormer Pro
TimingDiagrammer Pro

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