SynaptiCAD Big Feature List

SynaptiCAD was founded in 1992 to provide affordable high quality timing diagram editing tools. Since that time we have expanded our product line to include: VHDL & Verilog test bench generation, timing analysis, stimulus generation, Databook documentation, and Verilog simulation. SynaptiCAD products include:

Timing Diagram Editors

- **Timing Diagrammer Pro:** a timing diagram editor and timing analysis tool
- **WaveFormer Pro:** adds waveform translation and simulated signal support
- **DataSheet Pro:** a professional datasheet design environment that adds multiple timing diagram windows, logo image support, a OLE image linking, multiple print views, and style sheets.

Simulation and Debugging Tools

- **VeriLogger Extreme:** a Verilog simulator with unit level testing
- **BugHunter Pro:** a graphical debugging environment for VHDL and Verilog tools
- **GigaWave Viewer:** a waveform viewer and high performance waveform compression engine
- **Transaction Tracker:** a PSL/Sugar-based verification tools for viewing simulation data as higher level transactions instead of simple waveforms.
- **Verilog<=>VHDL Translation:** converts behavioral and RTL HDL models between the languages.
- **Gates-On-The-Fly:** a Verilog netlist schematic editor (graphical and batch-based editing and analysis supported). Also works with BugHunter Pro and GigaWave Viewer.

Test Bench Generation Tools

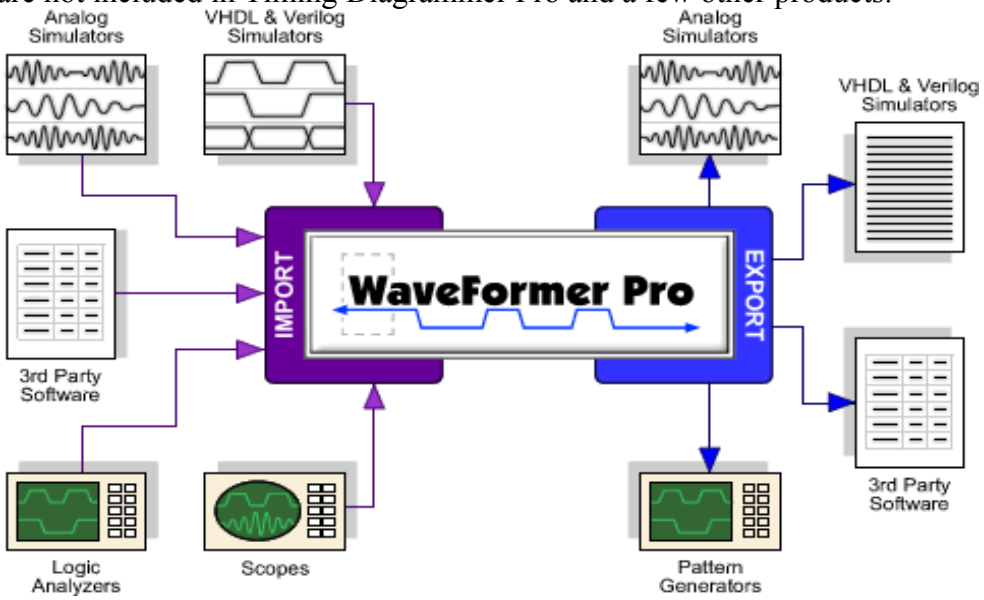
- **TestBencher Pro:** a VHDL and Verilog bus-functional model generator
- **WaveFormer Pro with Reactive TB Options:** creates single timing diagram VHDL and Verilog models that react to the model under test.
- **WaveFormer Pro:** creates single timing diagram VHDL and Verilog stimulus test benches.

Below is a partial listing of features contained in the SynaptiCAD Product line. The special starred features* are features that we have not seen in other currently available timing analyzer packages. Feature sets change, however, so we recommend that you get an evaluation of our product and try out the features. We think you'll agree that not only are SynaptiCAD's products the best priced timing diagram editors on the market, they are the most powerful and user friendly. Browse through the document or click one of the links below to skip to a section of interest.

Table of Contents

1. Waveform Translation Features

WaveFormer Pro, DataSheet Pro, TestBencher Pro and VeriLogger Extreme can import and export waveform data from over 50 different formats including simulators, pattern generators, and logic analyzers. Many of the import and export scripts are written in Perl and can be edited or modified by the customer to work for other simulators or in-house equipment. These features are not included in Timing Diagrammer Pro and a few other products.



Some Input Formats:

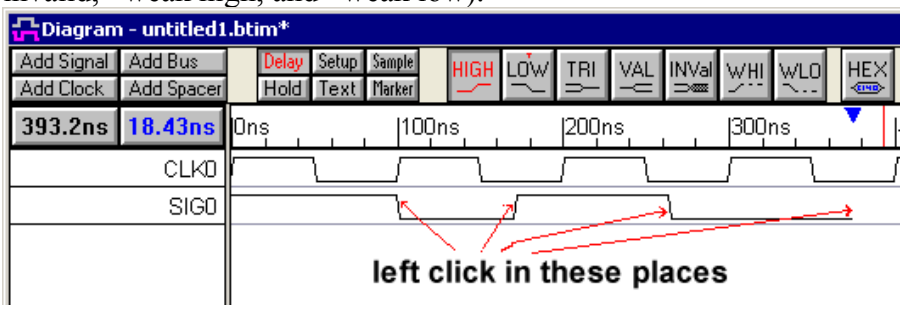
- Simulator formats: VCD, Speedwave VHDL, Aldec VHDL Waves, SPICE csd and tro, Workview WFM, Protel Advanced PLD,
- Static Timing Analysis Formats: Synposys Time Mill, Altera Timing Analyser Output, Xilinx Timing Analyser, Xilinx Speed File
- Standard Formats: TDML, BTIM, TIM, spreadsheet txt files, Chronoloty TD
- Test Equipment: all Tektronix and Agilent formats (8 different ones), Podalyzer Data

Some Output Formats:

- Simulation Formats: VHDL, Verilog, SPICE, HSPICE, PSPICE, HSim SPICE, Altera VEC, Mentor Quick SIM, ModelSim,
- Test Equipment Formats: all Agilent (HP) and Tektronix pattern generator file formats, STIL Test Vectors, PI-2005 Pattern Generator

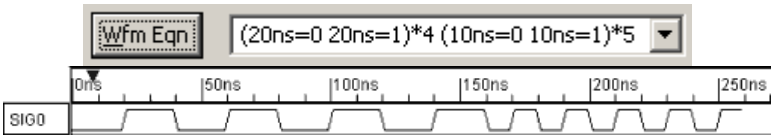
2. *Waveform Generation Features

* The timing diagram editor is always in drawing mode so left clicking on a signal will draw a waveform. The red state button controls the type of waveform that is drawn (high, low, tri-state, valid, invalid, *weak high, and *weak low).



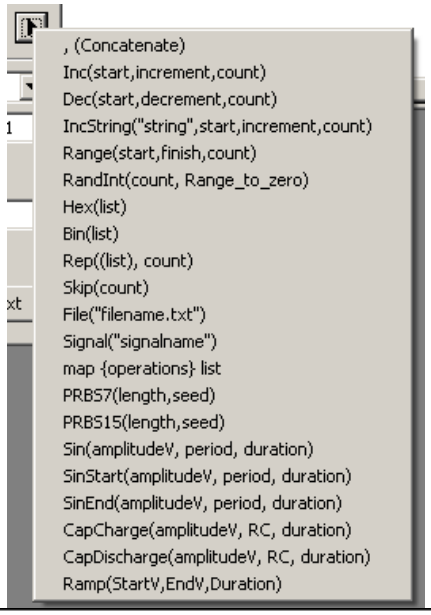
The timing diagram editors also include the ability to generate signal waveforms from equations and then label the states automatically. These features augment the drawing environment, and provide a quick way to generate signals without having to draw each signal transition. They also provide a way to generate signals that have precise edge placement.

- ***Waveform Equations** are time-based formulas that concatenate waveform sections to the end of a signal. They provide a quick way to generate signals that have a known pattern that is more complicated than a periodic clock.



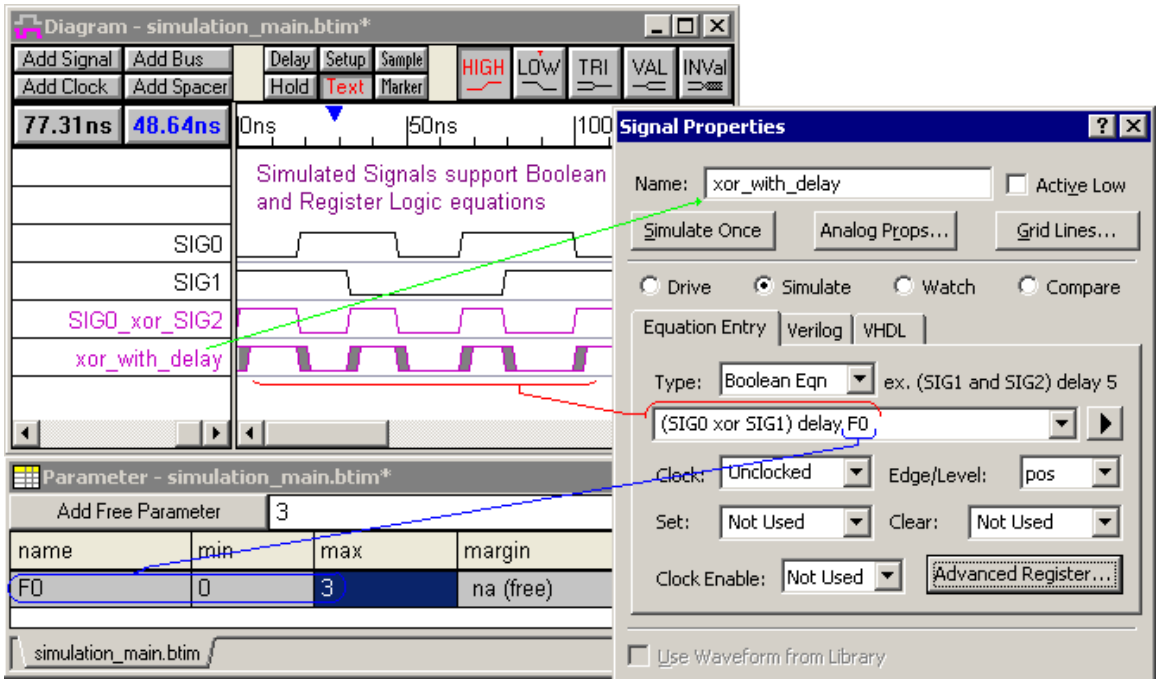
- ***Label Equations** provide a quick way to enter state values into digital counter signals and analog sine and capacitor discharge signals.
- To the right is a list of available labeling functions. Many of the functions can be concatenated to create complex label equations.

- Below is a signal that labeled automatically using the **Inc** equation.



3. *Simulated Signals

SynaptiCAD's simulation-enabled products (like WaveFormer Pro and DataSheetPro) contain a built-in Interactive HDL Simulator that is capable of simulating Boolean and registered logic equations. The simulator is interactive, because changes to the input waveforms cause the simulated waveforms to redraw. This feature greatly reduces the amount of time needed to draw a timing diagram, especially one that models gate level circuits.



- *IEEE 1364 compliant Verilog simulation engine that supports all major constructs of the language, including advanced features such as pin-to-pin timing and PLI interface routines.
- *Registered signals support flip-flops and latches. A point-and-click interface allows selection of edge triggering, level triggering, clocking signal, and timing parameter information.
- *The registers and latches have clock enable lines, and set and clear that can be synchronous or asynchronous. These features are particularly useful for designing divide-by-2 circuits and FPGA circuits.
- 64-Bit math classes allow the simulation of approximately 80s worth of time with 1ps resolution (or more time with decreased resolution). This means improved performance for users of large data sets captured by simulators and Agilent/Tektronix logic analyzers.
- Global* and individually definable options for timing parameters of registers and latches.
- Simulator supports min timing, max timing and min-max timing for gates, registers and latches.
- One-time and continuous* setup, hold and pulse-width time checking.
- Simulation is tightly integrated with built-in static timing analyzer.
- *Simulator supports behavioral constructs allowing the user to directly enter HDL code.
- *Vector (multi-bit equations!) support includes all normal math operators.
- *Support for tri-state gates and tri-state gating functions.
- *Support for multiplexing functions in equations.
- *Equations syntax supports an extended form of Verilog and VHDL equations that allows easier representation of combinatorial logic (multiple delays can be embedded into a single

expression and min-max timing information is much easier to express). The extended format is converted automatically to standard HDL that can be handled by third party tools.

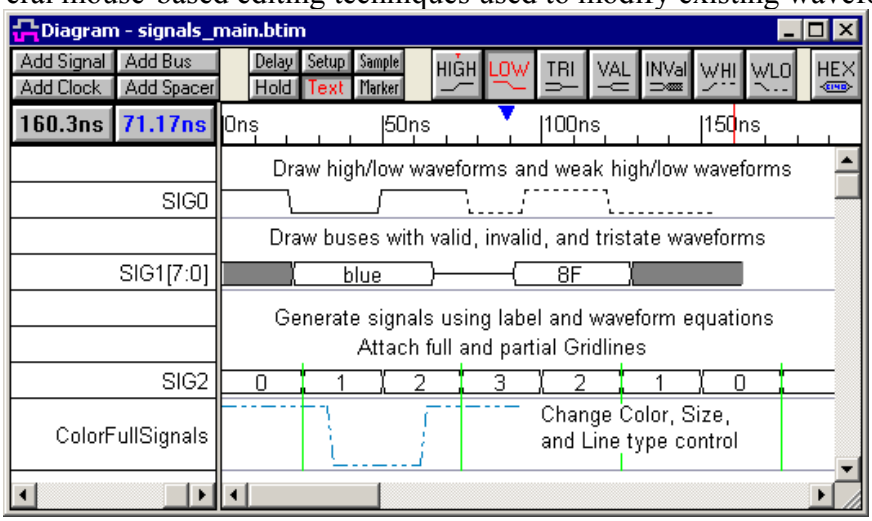
- Ex: Extended Verilog with multiple delays: sig2 = #5 (#10 sig0) & (#10 sig1)
- Ex: Extended VHDL with min/max timing variables: sig2 = sig0 and sig1 after Tpd would perform a min/max simulation of the AND gate using the min and max times specified for Tpd.
- *Ability to turn off continuous simulation mode and to perform one-time simulations on signals that are not continuously simulated.
- *Support for reconvergent fanout analysis in Boolean equations.
- *Signals can be switched back and forth between graphically drawn, and simulated modes.
- Below are some examples of Boolean equations:

3-input AND gate with a no delay	`SIG0 and SIG1 and SIG3`
3-input AND gate with a 20ns delay	`(SIG0 and SIG1 and SIG3) delay 20ns`
2-input AND gate using a delay parameter to define the delay time. Each edge of the simulated signal will have a gray uncertainty region that is the difference between the min and max times of GateDelay.	`(SIG0 and SIG1) delay GateDelay`
Tristate Gate	`EnableSig ? SIG0 : 'bz`
2-1 MUX	`S0 ? SIG0 : SIG1`
4-1 MUX	`S1?(S0?SIG0:SIG1):(S0?SIG3:SIG2)`
Signal Concatenation (Note: the simulated signal must have a proper MSB size to handle the result)	`{SIG0, SIG1}`
Concatenate bit slices	`{SIG0[3:0], SIG1[7:4]}`

- *User-definable gate primitives, modules, logic functions and math functions.
- *Support display of simulated vector results (virtual buses) in a variety of formats including binary, hex, and decimal.
- *Report window that allows the display and editing of HDL models generated by WaveFormer Pro, the results of simulation runs, and the execution of Perl scripts.
- Simulation status indicator on button toolbar that displays success/failure information about last interactive simulation. Makes it easy to spot when there is a mistake in your Boolean equations or Verilog code.
- MSB and LSB of multi-bit signals can be set directly in the signal name by bracketing this information (e.g. ADDR[31:0] sets MSB to 31 and LSB to 0). Changing MSB or LSB also changes display of signal name appropriately.
- *Report Window automatically displays vector stimulus and test bench files generated using the Export functions (Export menu options).
- *Macros can now be used in waveform segments and Boolean equations. This is a handy way to assign symbolic names to commonly used constant values such as instruction set assignments for microprocessors or constant values such as addresses on a bus.
- ***Waveform comparison provides comparison between individual signals or entire diagrams.

4. Editing Waveforms

There are several mouse-based editing techniques used to modify existing waveforms.



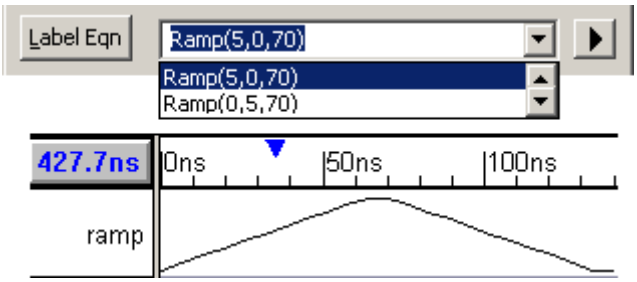
- **Editing Signals**: *Left mouse button always draws and edits signals
- Drag-and-drop signal edge transitions individually using the left mouse button.
- *Move all transitions on one signal by holding the <1> or <2> key while dragging. The <1> key moves all edges to the left, and <2> moves edges to the right.
- *Move multiple transitions on different signals by selecting with <CTRL> and dragging.
- *Insert Segment into signal by clicking and dragging within a signal.
- Change a segment's graphical state by selecting it and then pressing a state button.
- Delete part of a signal by selecting it and typing the delete key.
- *Automatically snap the ends of waveforms to a common time using a Marker
- ***Snap to Edge Alignment Grid** allows quick placement of edges which line up with clock edges or other signals.
- **Snap signal transitions to the closest clock edge** by setting the signal's clocking signal
- Specify the exact position of an edge by using the Edge Placement dialog
- Lock an individual edge or all edges on a signal so that the edges cannot be dragged or shoved from its current position.
- ***Active Low Signal Names** have a bar (line) on top.
- **Copy/Paste** Signal Waveforms and attached parameters and text.
- ***Block Copy Waveform sections** in the timing diagram (horizontally in time). Possibly the all-time most requested feature. This makes it easy to repeat a section of waveforms (e.g. to create multiple copies of a write cycle on your diagram).
- Signals can be hidden and moved.
- Color coded signals indicate direction.
- Each signal transition can have its own multiple delay reconciliation function (delay reconciliation functions allow the user to specify how multiple delays force a single transition.

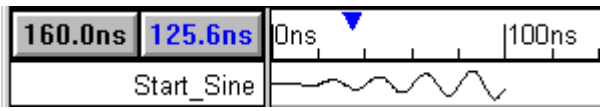
5. Analog Signal Support

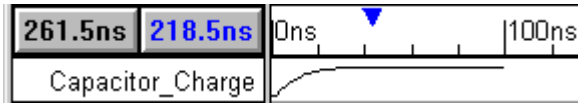
The analog features allow analog signals to be imported, exported, created, and manipulated. Digital signals can be converted to analog signals and vice versa (similar to the way analog-to-digital converters operate).

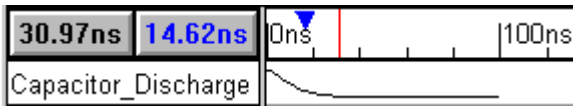
- ***Analog Signals** can be created and displayed as analog waveforms or digital buses. Each signal has a complete set of analog properties that control how digital values are converted into analog values. If a signal has a radix of real, the values of the signal will be exported directly as voltage values. If a signal has a radix except real, an internal Digital to Analog converter will use the bus size and the logic voltage level settings to convert the digital waveform value into an analog value.

- ***Sine**, **Capacitor**, **Ramp**, and **Exponential** waveforms can be automatically generated using State label equations.

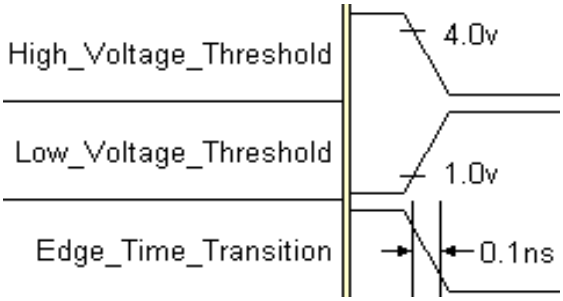






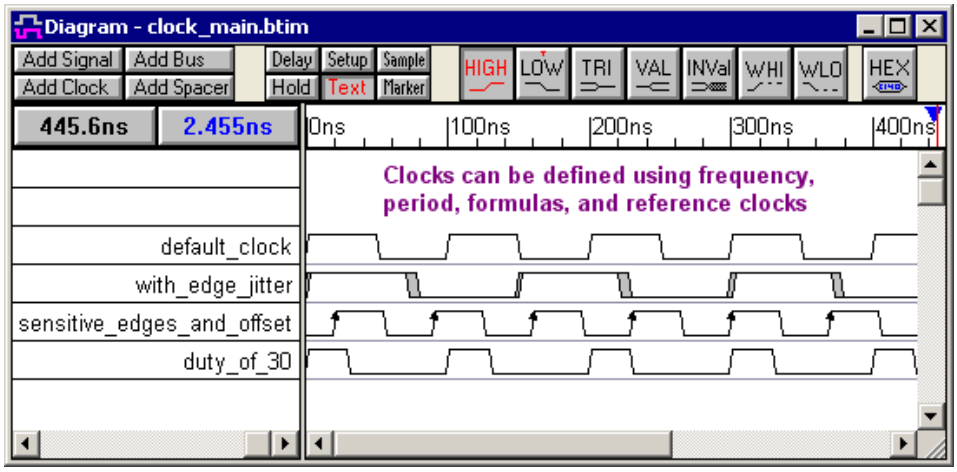


- Text Objects that are attached to edges can be made to show the high and low voltage thresholds, and the edge time transition points. The signal's analog properties determine the placement of the marking lines and the values of the properties.



6. Clocks

Clocks draw themselves based on their attributes: period of frequency, duty cycle, edge jitter, offset and other parameters. Clocks can also be related to other clocks by creating master clocks or by using formulas that reference another clock's attributes like period, offset and jitter.

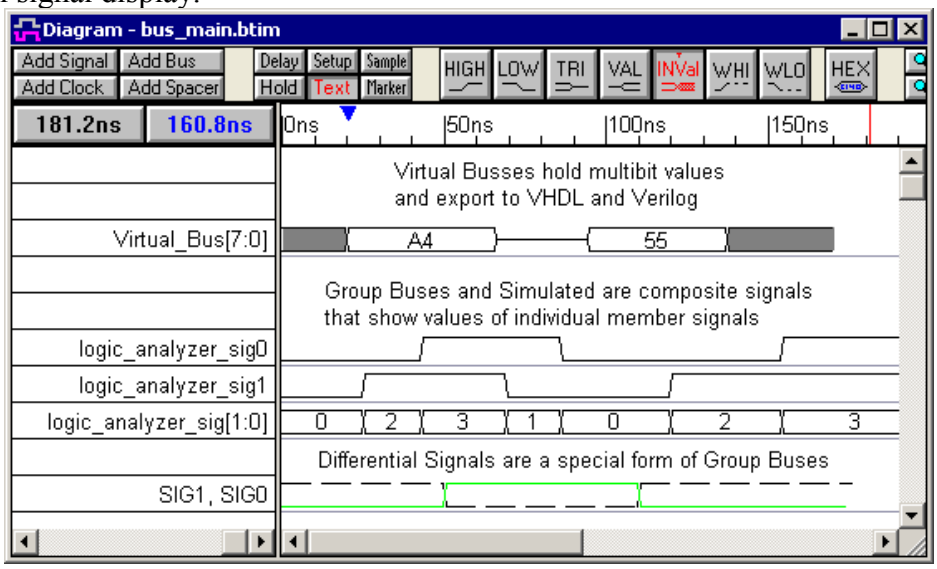


- Create a new clock by using the **Add Clock** button
- Convert a VCD or logic analyzer signal into a clock using the right click menu.
- Double click on the clock waveform to open the ***Edit Clock Parameters*** dialog which is fully interactive and updates clock as you change attributes.
- Insert/Delete clock cycles by selecting a clock edge and pressing the <Insert> or <Delete> keys.
- Exact placement of a clock edge found by double left clicking on the clock edge.
- Draw Grid from clock edges (specify color, style, and grid spacing).
- Three ways to define the **Clock Period or Frequency**:

    - **Use a fixed time or frequency.**
    - **Use a time formula** based on other clocks and parameters This is particularly useful for describing circuits in which the clock frequency and delay values change depending on the speed grade of the part being used or for phase-locked loop (PLL) frequency multiplier circuits. By storing a clock frequency in a parameter, and referencing that parameter in the frequency box of the clock, the entire diagram can be changed by loading in a different parameter library for each speed grade.
    - ***Use a Reference Clock** which tightly relates two clocks and is the most accurate way to model a clock divider implementation. This also correctly models delay correlation effects between the reference clock and the sub-clock.
- Use formulas to specify the clock offset, and rising and falling edge jitter.
- Use extended state information to label clock cycles. The extended state information automatically centers itself within the cycle and adjusts as you change clock frequencies.
- **Modeling Clock Skew with Delay Correlation**: Datasheets for clock tree buffer ICs often include a timing skew parameter that can be used to compute the delay correlation between the buffer gates inside the IC. To take advantage of the skew information, you can create a correlation group with the calculated delay correlation value that contains the clock buffer delays. This delay correlation group will automatically account for the clock skew in all the timing calculations related to the clocks.

7. Buses and Differential Signals

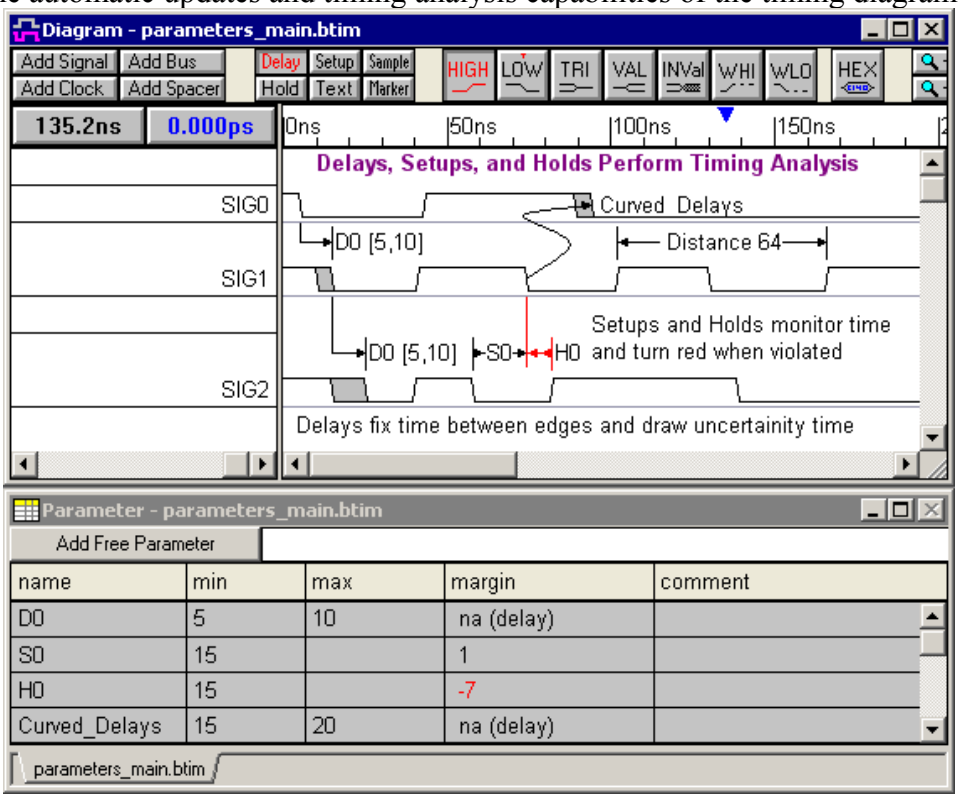
A bus is a multi-bit signal. The timing diagram editor supports three types of buses plus differential signal display.



- **Virtual Bus** is a single signal defined as multiple bits. This is the most common bus and the easiest to work with because all of the normal signal-editing techniques work on it.
    - *VHDL and Verilog stimulus generation supports virtual bus export.
    - *Set virtual bus size by double left click on signal name to open the Signal Properties dialog.
    - ***The built-in functions for State Label equations** enable you to generate most bus sequence types, but it is also very easy to add your own unique functions (written as short Perl routines). For example, the following equation would create a bus signal named CNTR that starts counting from 64 by fours for 100 clock cycle, repeating the entire sequence four times: **(CNTR Rep(Inc(64,4,100),4)**.
- **Group Bus** displays the aggregate values of its member signals. This is handy way to manage lots of single bit signals that have been imported from other sources.
    - *Compress several signals into a bus signal, or create a new bus and its member signals.
    - *Draw all the member signals of a bus at once by drawing on the bus
    - *Edit all the signals of a bus at once by left clicking on a bus segment then left clicking the HEX button and typing in the new state. (Edits just like signals)
    - *Switch between hex or binary display using Options/Drawing preferences
    - *Insert a new bus segment by double left clicking on the bus
    - *Hide member signals on Bus merge option
    - *Bind and UnBind member signal transitions inside Buses
    - *Align signals to a bus edge
- **Simulated Bus** is a simulated signal defined as a concatenation of it member signals. This is primarily designed for the testbench products so that both a member signal and the whole bus can be passed to models as needed.
- **Differential Signals** are two-bit group buses that display a superimposed image of the member signal waveforms. Supports both **Analog and Digital waveforms**.
- **Convert Between Bus and Signal Types** using the right click menus.
- **Use Symbolic State Names** instead of numeric state values.

8. Delay, Setup, and Hold Parameters

Delay, Setup, and Hold parameters actively move and monitor signal transitions. They provide the automatic updates and timing analysis capabilities of the timing diagram editor.



- **Delays:** Force edges to a fixed distance.
    - **Delays Add Up:** Delays define a timing path through a circuit. As the timing path goes through each gate the delay uncertainty regions will add together.
    - **Delays are color coded** to indicate which edges of the transition they control.
    - *Min Only and Max Only delays that only affect one edge of a transition
    - Multiple delays can force a single transition (4 reconciliation methods available).
    - Toggle switch for color coding of delays for perfect black and white printing (View\Show Critical Paths…).
    - Delays automatically **remove common delay** to correctly calculate reconvergent fannout.
    - * Delays can be grouped into **correlation groups** to remove uncertainty ranges for related delays.
- **Setups and Holds:** Monitor time between signal transitions.
    - Add Setups and Holds by selecting the ***data signal*** and **then** right clicking on the ***control signal***. The setup or hold points to the control signal.
    - Setups and Holds turn Red to indicate a violation
- **Drawing and Editing Parameters**
    - *Press the ***Delay***, ***Setup***, or ***Hold*** button then use ***right mouse clicks*** to add the specified parameter. This frees the left mouse button so you can always draw and edit signals.
    - To Edit double click on a parameter in either the diagram or parameter windows.

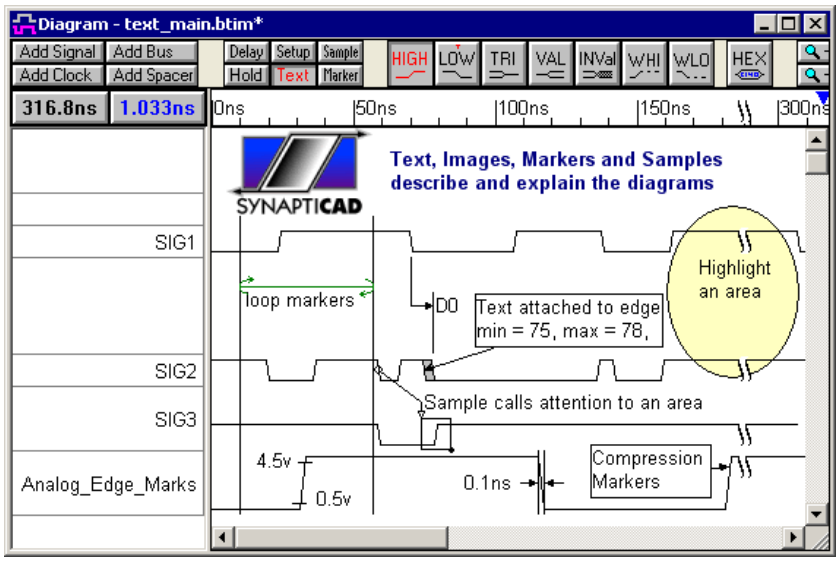
    - *__Move a parameter to a different edge__ by selecting it and then dragging the black handle to a different edge.
    - *__Repeat Parameters__ across the diagram using the Repeat button the *Properties* dialog
    - **Automatically share Parameter Data** between different parameters that are attached to the ***same signals*** and the ***same types of edges pairs***.
    - *Share Parameter Data by naming the parameters the same name. This makes it easy to share/unshare parameter values (this can be very tedious in other tools).
    - *Smart Parameter Lookup in the Parameter Properties dialog box allows you to easily use data from existing parameters by using an existing parameter's name.
- Most of the **display settings** for parameters are contained in the *Properties* dialog.
    - **Curved Parameters** instead of the right angle display are fully editable.
    - **Outward Arrows** can be used to indicate measurement.
    - **Display any parameter property or custom string** using control codes in the customer label box (i.e. parameter labels like "tpCK2O [10,20]").
    - ***Realistic Data Book Parameter Names** like t_{pd} supported with subscript, superscript, bold, and italic formatting.
    - Control codes can also be placed in text strings os that you can put edge times in your text that automatically update.
    - Drag & drop parameters to a **new vertical position**, including positions between a new pair of signals.
- Move parameters in spreadsheet using drag & drop
- Adjustable column widths in parameter spreadsheet
- Hide and delete in parameter window
- Selectively display all objects of a given type: delays, setups, holds, and text
- *Drag transitions from either min or max edge for more control over edge placement.
- Transitions can have overlapping uncertainty regions (option can be turned off).
- **Parameter Filters:** Control what you see using the filter dialogs to filter signals and parameters - use powerful features within testing to keep your viewing area simple.

Add Free Parameter	f(a,b)	
name	min	max
f(a,b)	a+b	2*a-b
g(in)	f(in,4)	f(in,(4+F0.max)/3)
h(d)	g.max(d)+f(3,5)	g.min(f(4,5))

- *Delay, Setup, and Hold timing parameters can be referenced in other parameter formulas (i.e. **D1.max = 2*D0.min**).
- Free parameters: Parameters not attached to edges that can be used in other parameter formulas.
- *Different formulas can be given for MIN and MAX parameter values to model complex timing relationships.
- *Can use .min and .max attributes to access either value of a parameter in any formula. This allows you full control of formula evaluation unlike other timing analyzers which generally force you to accept their interpretation of which value to use. Also prevents the need for non-standard mathematical operators.
- *Easy-to-use formula and data entry that doesn't require annoying brackets and commas.
- "Display time units" setting so that you can enter values at a convenient level and still have the resolution of a smaller "base time unit".

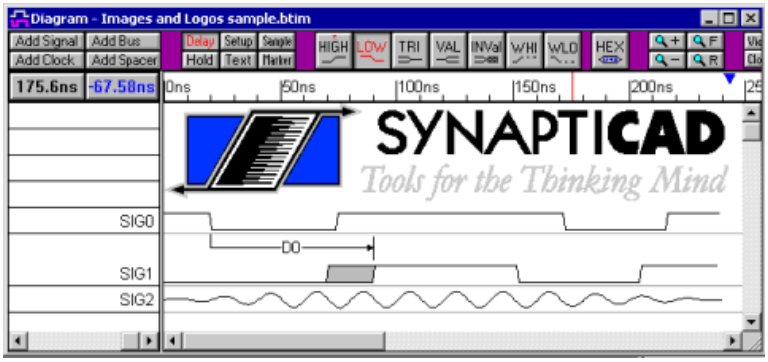
9. Text, Markers, and Samples

Text, Marker lines, and Samples can be used to annotate the timing diagram. Special events can be called to attention by attaching a text to the edge. Special States can have a sample describing the activity. Text objects can be placed anywhere with complete font, size, and color control. And in DataSheet Pro images (like logos) can be imbedded directly into the timing diagram.

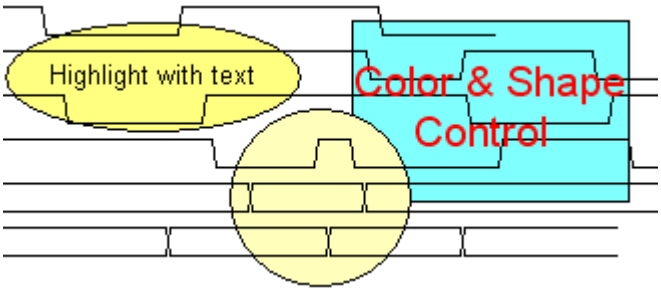


- **Text annotation:** Add comments and titles anywhere in your timing diagrams.
    - Press **Text** button then right click to add text objects
    - ***Text placement grid** makes it easy to align multiple lines of text.
    - ***Keyboard "nudging"** with the arrow keys to move text in any direction.
    - **Multi-line text blocks** can be added by editing an existing text object.
    - Copy and paste keyboard shortcuts (CTRL-C, CTRL-V) can be used to copy text to or from a word processor.
    - Text objects can be placed at a **fixed time** or **attached to an edge**.
    - Text can be centered inside a signal, bus, or clock segment (especially useful for documenting multiple clocks of a bus cycle or multi-phase clock systems)
    - Individual font and font color control for each text object.
    - *Support subscripts, superscript, bold, and italic formatting (CTRL-D, CTRL-U, CTRL-B, and CTRL-I).
    - Drag & Drop to move text.
    - Double left click to edit text.
    - Use right mouse button in text mode to add text.
    - Dynamic substitution codes can display information about the edge that the text is attached to.
    - Choose between opaque and transparent backgrounds
    - **Text on Hidden Signals:** Normally, hiding a signal will also hide the text and grid lines attached to the signal. However, sometimes it may convenient to use a signal just for holding text or grid lines, but otherwise that signal is unrelated to your circuit design and does not need to be displayed. The checking View > Show Hidden Text menu, then hiding the documentation signal will allow the text to continue to be displayed even though the signal is hidden.

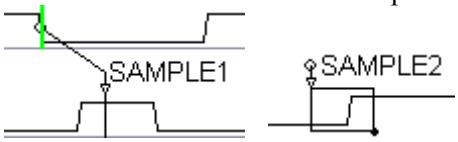
- DataSheet Pro allows images and company logo files to be embedded into a timing diagram. Once the image is saved by DataSheel Pro, it can be viewed in any of SynaptiCAD's timing diagram editor products including the free WaveViewer product. The link to the image file is stored in a Text Object and has the same kind of attributes as a normal text object that allow the image to be locked to a particular place on the screen or attached to a particular edge or signal.



- Text Objects can be used to highlight an area on the timing diagram.

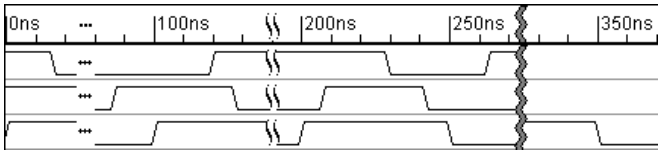


- **Samples:** Graphically indicate a point at which a signal should be sampled (e.g. latched or registered). See the TestBencher Pro feature section for specific code generation properties.



- Markers are vertical lines that display their placement time in the timing diagram. Once a marker is added to the timing diagram, its behavior can be altered so that it compresses time, mark the end of the diagram, create a loop in the diagram, or call an HDL code segments

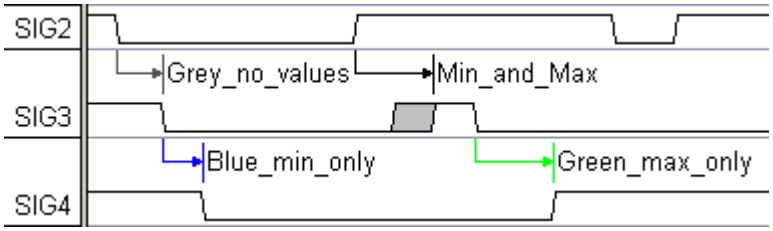
  - Markers can display any of their properties using control codes
  - Markers can be attached to an **absolute time** or an **edge**
  - Edge lines for Markers optionally show the attached edge
  - Display Signal States with Markers
  - *Useful for generating conditional burst type transactions



10. Advanced Timing Analysis Features

The advanced Timing Analysis features are included in all the products that contain a timing diagram editor.

- ***Delay Correlation:** SynaptiCAD's timing diagram editors have the capability of specifying a correlation percentage between timing delays. This lets you account for the correlation in delay times between gates on a single chip. For example, the absolute delay for gates on a FPGA might be specified in a datasheet as 5-10ns (min/max). This min/max delay variation is due to variations in the particular batch lot of the chips and potential variations in operating temperature. However, the maximum delay difference between any of the gates on a given chip is much smaller than the worst case given in the datasheet (all the gates came from the same lot since they are on the same chip and they are operating close to each other in temperature). To model this in WaveFormer, you can specify the min/max delay from the datasheet and a correlation percentage that indicates how much variation there can be between the correlated delays (100% correlation meaning that the delays on all the gates will happen at exactly the same time and 0% meaning the delay times are randomly distributed as if they were gates on different chips).
- **Reconvergent Fanout:** Automatically removes common signal delay uncertainties from setup and hold margin and distance calculations.
- **Multiple Delays** on a single transition:
    - Four methods of reconciling multiple delays: earliest transition, latest transition, min uncertainty, max uncertainty.
    - *Ability to set the default reconciliation method for multiple delays.
    - ***Visual display of min/max critical paths** using color coded delays to indicate which delays are forcing the min and max edges of a transition. This type of critical path display is necessary in diagrams where multiple delays drive a signal transition. The colors are: Gray = none, Blue = Min only, Green = Max only, Black = both min and max.



    - ***Ability to specify minimum uncertainty on a transition** (from Edge Placement dialog). If no delays cause an uncertainty greater than the transition's minimum uncertainty, the transition will be given its minimum uncertainty value.
    - ***Min Only and Max Only Delays:** delays that only affect one side of a transition.
    - *Delays turn red when violated: Especially useful for determining dominant delays when multiple delays are forcing an edge.
    - Setups and holds turn red when their margins are violated.

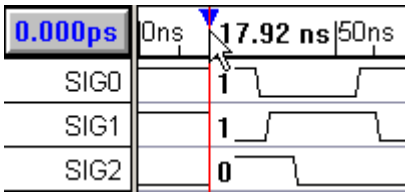
11. Measuring Time and State Values

*All the SynaptiCAD timing diagram editors feature a **Modeless Measurement** environment so that relative and absolute measurements are always displayed on the screen using the black and blue time buttons. There is no special measurement mode that you have to get into and out of and no clunky cursors to drag around.

- ***Relative Measurements (distance between two objects):** Get the relative time between two objects with only two mouse clicks. Left click on the first object. This moves the blue delta mark to that position. Now the blue readout/button above the signal names will display the distance between the blue delta mark and the mouse cursor. If the left mouse button is pressed down on an object like a signal transition then that object can be dragged while the delta display shows the relative time between the objects.

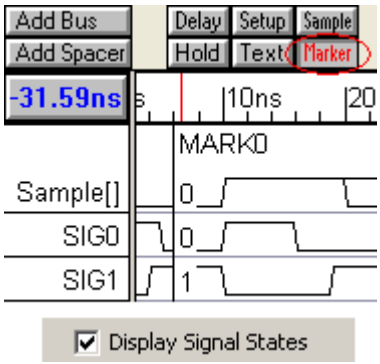
- **Absolute Measurement with the mouse:** The time display always shows the position of the mouse in the diagram window. To find the location of an object in the diagram window, place the mouse on top of the object and read the time display.

- Temporally **display Signal States** by clicking in the time line.



- Permentaly **display Signal States** by using a Time Marker and setting the Display Signal States.

- Permentaly **display an Edge Time** by using a Time Marker attached to an edge and set the Display label to time.



- **Exact Absolute Measurement of an Edge:** Double clicking on a signal transition will cause the "Edge Properties" dialog box to display the min and max time of the transition.
- **Display the position or uncertainty of an edge:** Get into the Text mode. Left click on an edge, right click to open an edit box. Enter %m, %M, or %u control codes to display min transition, max transition, or uncertainty region.
- **Display the distance between two transitions:** Add a delay, setup, or hold parameter between the two transitions. Double click on the parameter to open the "Parameter Properties" dialog box, and choose distance radio button.
- **Generate a Timing Analysis Report** by using the **File > Save Timing Diagram As** menu and then choosing Timing Analysis Report as the type of file. The generated report will be written to a file and also be displayed in the report window.

12. Usability Features

The Usability Features are included in all the products: Timing Diagrammer Pro, WaveFormer Pro, DataSheet Pro, BugHunter Pro, and TestBencher Pro.

- **Multiple Undo and Redo:** Undo up to 20 previous drawing and editing actions. The **Undo Delete** menu option remains, so deletes can be undone without changing the multiple undo/redo buffer.
- ***Modeless Drawing:** Ever wonder why some CAD programs are mode intensive? To perform even the simplest editing and drawing you have to be in the correct mode. SynaptiCAD's timing diagram editors allow you to draw and edit waveforms no matter what mode you happen to be in.
- ***Modeless Edit Bus State Dialog**
- ***Group Edge Shifting** allows moving all edges in a signal. Holding down either the "1" or "2" key while dragging a transition causes all the transitions to the right or left of the selected transition to also be moved. Holding down both keys causes all the edges in the signal to move together.
- ***Centered Zooming** about a selected edge and regular zooming from the center of a diagram.
- **Search for a specific signal name, parameter name or string**, in any window, by using the search box on the program button bar.

- ***Object Oriented Drawing Environment:** SynaptiCAD's timing diagram editors use an object-based drawing environment. This means you will be able to extrapolate most functions if you know how to do something similar. For instance, one way to delete a signal is to select it by left clicking on the signal name then pressing the delete key on the keyboard. Similarly, to delete a delay object, select it with the left mouse button and press the delete key.
- ***Optimized code (fast drawing, scrolling, file loading, and program loading):** After our timing diagram editor program was written, designed and debugged we went back and made it better. Many Windows programs are slow, but we took the time to make ours fast. This was especially critical to support the file translation capabilities of WaveFormer as it has to be able to handle diagrams with hundreds of signals and several hundred thousand signal transitions.
- ***Drag & Drop File Load:** From File Manager or Explorer you can drag a .btim file (normal output file) and drop it onto a diagram or parameter window to open the file. This is helpful if you have a lot of timing diagrams and would like to view them in rapid succession (You can also double click on the first one to start WaveFormer).
- ***** **Binary and Text files supported:** The native file format for the timing diagram editor is a fast loading binary file called BTIM. The timing diagram editors can also save files to a fully Text based format, TIM, that can be easily read by or written by other software programs.
- **File History List:** The File menu has a history list of the last four files that were used. This helps you quickly load your current project. Left click on a file in the history list to open that diagram (or use ALT-F1 to open the last file you worked on).
- **Intelligent Windows:** The Diagram and Parameter windows remember their size and location the last time the program was run. This means that you don't have to size and move the windows each time you run the program. Fonts, colors, and window specific options are also remembered.
- **Proportional Scroll Bars:** The thumbs on the scroll bar are proportionally sized to indicate how much of the window is being viewed.

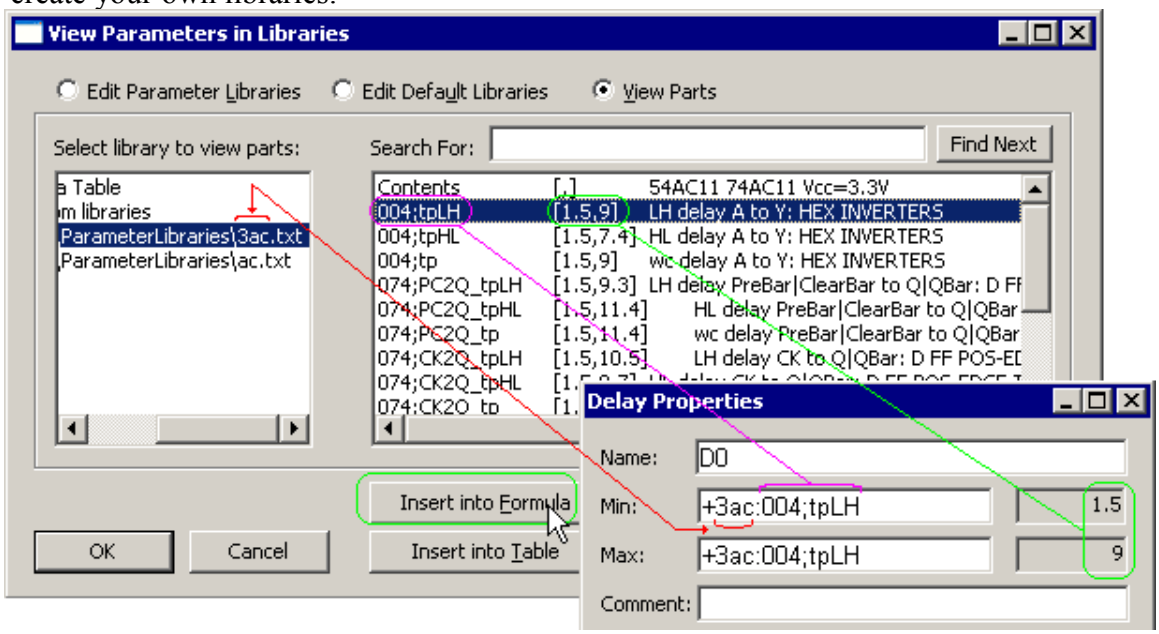
- ***Pushed in Buttons:** The buttons in the editor looked pushed in when they are activated. No squinting necessary to detect that dotted gray box around a normal Windows' button.
- ***Space Efficient Status bar and Quick Overviews:** Nobody wants to read the entire help before they use a program for the first time so we have status bars and two short overviews to help new users get started. Our status bar is displayed on the window title bar to save on screen real estate.
- ***Convenient Naming** of Buses, Signals, Clocks, & parameters (Right click on add or mode button to change the default naming prefix). This makes it easy to create several objects with iterating names (i.e. tp1, tp2, tp3, etc.).
- ***Turn on/off State Button toggling.** Double click on a state button to turn off toggling. Click on another state button to turn toggling on again. Makes it easy to draw signals consisting of a number of valid segments.
- **Lock or unlock all the edges** on user-selected signals by choosing menu option Edit > (Un)Lock Edges of Selected Signals.
- **Reactive Cursor Indicates Editing Operations:** The cursor changes shape to indicate the different editing options available for particular objects.

object	cursor	action
parameter	up-down arrow	move parameter up or down
parameter handle	pointer	drag handle to new edge
text	four-way arrow	drag or nudge in any direction
marker or edge	left-right arrow	drag or nudge left or right
all other objects	cross hair	regular editing and drawing

- ***Edit Box History Lists:** Many edit boxes are equipped with permanent history lists that store information from session to session. History lists save the user from retyping previously entered information. History lists are stored in the timing.ini file in the Windows directory and can be pruned and rearranged in that file (be sure the program is not running while editing this file or changes will be lost when program is closed).
- ***Compact dialog boxes** allow maximum use of your screen real estate (great for laptops).
- ***Context sensitive help** for dialogs provides immediate reference for features and links directly to online help
- ***Auto Save and Recovery of Data:** Timing diagrams will be temporarily saved at the indicated interval. If the program is prematurely terminated, then the next time it is launched it will reload the temporary file so that you can choose to use this data or revert to the original file. This is product specific feature, so you must launch the same program as the program that was running during the crash to recover the file. For example, if you were running TestBencher before your operating system crashes, then you must run TestBencher (not WaveFormer or other products) to recover the data.

13. Parameter Libraries and Merging Diagrams

All the timing diagram editors include support for Parameter libraries. Parameter Libraries are free parameter files that can be shared by several timing diagram projects. They contain the timing parameter information of components. The timing diagram editor ships with several standard libraries that contain over 10,000 timing parameters, and it also supports the industry standard TDML on-line component information. You can also use the timing diagram editor to create your own libraries.



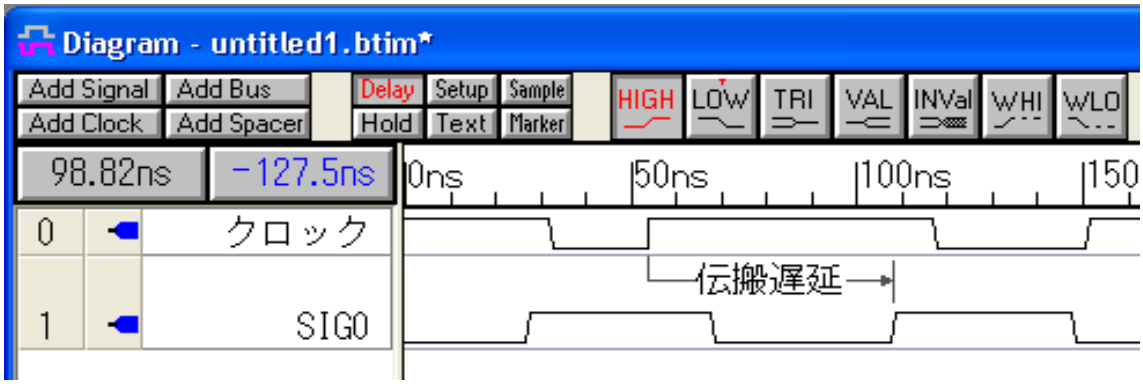
- Ability to browse part libraries and insert parts directly into project.
- Reference parts without including them in the project so that when the libraries change your diagrams are automatically updated.
- *Copy referenced parameters into your project to make it self-contained. This makes them easy to move and freezes them so that future library changes will not disturb your project.
- Update project from libraries so that self-contained projects can be updated if necessary.
- *Easy part referencing. Insert library parameter names directly into formulas by pressing the library button or F3 key and selecting parameter from library parts dialog. Parameter names are placed at current cursor location.
- *Faster Library Specifiers: The Edit Macro dialog finds the library specifiers that are defined for the current project and displays them in the Value drop down list box. This simplifies and speeds up the process of switching between libraries.
- Hide parameters in parameter spreadsheet window.
- Able to import & export library parameters to spreadsheets in tab separated value format.
- Able to read Chronology(R) libraries.
- *Easily create custom libraries by saving free parameters from any project.
- Macros allow you to substitute one string or character for another in formula evaluation making it easy to quickly switch vendor libraries and parts.
- Library files can be placed in different directories and even on different machines so networked users can share a common set of library files.
- *Merge diagrams with a special dialog that helps you handle parameter conflicts.

14. Documentation Features

In addition to having superb timing analysis features, SynaptiCAD's timing diagram editors also have the most documentation features for producing print quality timing diagrams from your design diagrams. Most of these documentation features are included in all the products: Timing Diagrammer Pro, WaveFormer Pro, DataSheet Pro, VeriLogger Extreme, and TestBencher Pro.

Realistic Data Book Display Features

- * **Realistic Data Book Parameter Names** like t_{pd} supported with subscript, superscript, bold, and italic formatting.
- *All text objects and parameter comments support subscript, superscript, bold, and italic formatting.
- *Signal names with an over bar (line on top) indicate active low signals.
- *Edge placement grid makes it easy to line edges up with clocks or other signals edges.
- *Text placement grid makes it easy to align multiple lines of text.
- *Group Edge Shifting allows moving all edges in a signal for quick editing of the timing diagram. Use CTRL and SHIFT keys individually or in combination while dragging and dropping the selected edge.
- ***Japanese and other non-English Fonts** are supported.

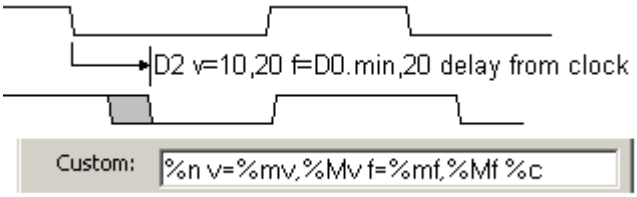


- Signal ends can be snapped to a marker. This makes it easy to end all signals at a common time.
- *Data sheet quality 0-1ns setups and holds. Data sheets often contain many 0ns setups and holds. WaveFormer Pro represents small setups and holds as two horizontal arrows pointing to a center line for a more professional display.
- ***Time Breaks that compress time:** Time breaks are spcial markers that can compress time, the section of time still exists, but will not display on the screen. Time breaks can be used as an aesthetic graphical display, or as a true time compression marker. There are three graphical time break styles (dotted, curved, and jagged) that emulate the most common time breaks used in data books.
- ***Indicate Loops using paired Marker Lines**
- ***Highlight Areas with Text Objects**: The objects can have different shapes and colors and be attached to time or to an edge.

Parameter Display Features

- Drag & Drop control over parameter location in your timing diagram.
- Control which attribute a parameter will display like: name, min/max time, min/max formula, margin, distance, or comment. Both global and individual object control.

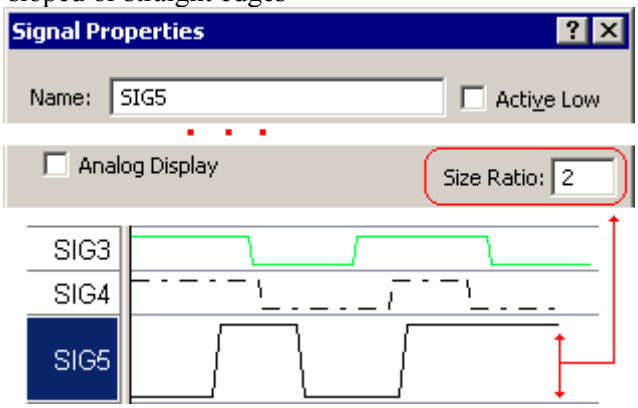
- *Custom Parameter display: if the normal parameter output is not exactly what you want then design your own custom string. Use control codes to reference a parameter's values inside the custom string. For example: **D0's delay time = %m,%M** custom string would replace %m with the min time and %M with the max time of delay D0. The rest of the string would display as typed. Control codes are available for all parameter attributes. Both global and individual object control.



- Curved parameters
- Samples that indicate special areas to notice in the diagram.

Signal Display Features

- *Signal Names can be displayed with an over bar or line on top for active low signals.
- Control the width of signal name window by dragging & dropping the bar separating the signal names and signal waveforms (nice for printing and image creation).
- Signals can be displayed with either sloped or straight edges
- *Control pixel slant of sloped edges
- *Control waveform line thickness
- Control the type line for waveform
- *Control waveform color
- Control the height of the signal
- Add arrows to the transitions to indicate edge sensitivty



- *Spacer signals improve document appearance (great for titles at top of diagram). Spacers allow you to add extra space between signal names without having excess signal separator lines drawn.
- *Control codes can also be placed in text strings so that you can put edge times in your text that automatically update.
- Signal ends can be snapped to a marker so that all the signals in a diagram can easily be made to end at the same time.
- Right justify signal names using the Drawing Preferences dialog.
- **Signal Filters** control what you see using the filter dialogs to filter signals and parameters - use powerful features within testing and keep your viewing area simple.

Font and color control

- Control the fonts and color of objects at three different levels: global for entire program, at the window level, and for individual objects.
- *Control of global default font that is used by all windows unless individually specified. This also makes it easy to change the font of all your text objects at once.
- *Control the font used by individual windows: button-bar, header, diagram, label, and parameter windows.

- Control the font used by individual text objects.
- Control color for an individual signals or make all signals rainbow colored.

Standard File and Image File Support

- **Support for TDML:** Over the next two years, on-line data sheets are going to augment or supplant printed data books. TDML (timing diagram markup language) is the timing diagram and timing parameter format recommended by the Si2 ECIX committee involved with defining the data sheet standard. With TDML, you will be able to view on-line data sheets (supplied by semiconductor manufacturers) in a browser-like environment, then automatically launch WaveFormer Pro to display and manipulate the timing information. SynaptiCAD has been working with Si2 since November of 1996 to define the TDML standard. We expect to see the first on-line data sheet sites in early 1999. Keep checking our web site for updates on the latest TDML information.
- *Scaleable **FrameMaker MIF** images. Once our MIF images are imported into FrameMaker you can grab the edge of the image and scale the image as desired.
- *Ability to set horizontal size of **FrameMaker MIF** images. Useful when generating multiple MIF images of the same size.
- *Five vector image formats for creating publication quality documentation.

    - MIF files for FrameMaker (editable from inside FrameMaker)
    - *EPS files and support for imbedding image previews (good cross-platform format)
    - *CGM metafiles (editable images for Microsoft Office)
    - *EMF enhanced metafiles
    - WMF metafiles (these are written to a file and also put on the clipboard so you can use the Edit\Paste command to insert image into MS Word)
    - SVG Scalable Vector Graphics
    - TIFF (DataSheet Pro only)
    - PNG (DataSheet Pro only)

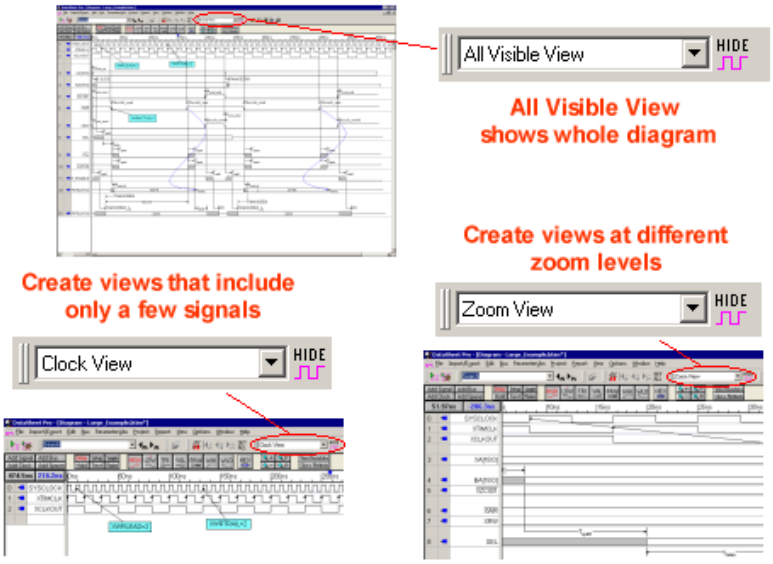
Image Export & Printing Features

- *"Smart" Print Settings. The default range for printing the timing diagram window is the **End Diagram Marker**. If there is no End Diagram Marker, then the timing diagram window is printed to the farthest non-repetitive signal edge.
- Copy waveforms to clipboard (bitmap format used by virtually all Windows programs).
- Copy timing parameters to clipboard.
- *Copy to clipboard is WYSIWYG.
- Printing: Horizontal and vertical scaling of your entire diagram. Allows you to fit your diagram on a single page even if you have a large number of signals. Also allows you to scale your entire diagram including fonts.
- Control of header and footer text.
- Control of printer margins.
- Scaled to page printing allows you to autoscale waveforms to fit on a given number of pages.
- Export timing parameters to all major commercial spreadsheets.
- DataSheet Pro supports

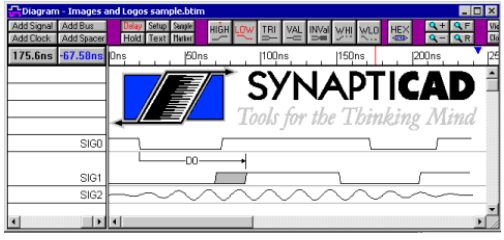
15. DataSheet Pro Documentation Features

DataSheet Pro provides a standardized exchange mechanism for designers and technical documentation specialists. This solves many of the most serious problems associated with creating IC data sheets by eliminating the need to reenter data, avoiding misinterpretation of specifications, and keeping technical data synchronized between engineers and the published documentation. Besides importing timing diagrams from engineering design tools, DataSheet Pro can also create timing diagrams using its professional editing environment.

- *Built-in timing diagram editor with multiple timing diagram display
- ***Project Management** allows multiple timing diagrams to be listed in the project window, providing easy access to all the diagrams in a particular design. Double clicking on a file name opens the timing diagram for editing.
- ***Style Sheets** make it easy to ensure that a set of timing diagrams conforms to a departmental standard without enforcing the style on the diagram creators.
- ***Multiple Views** let the user to store the settings for multiple pictures (images) taken from a single timing diagram.



- ***Web Compatible and Vector based Image Creation.** Datasheet Pro supports additional formats like PNG, TIFF and JEPG that give documentation specialists the ability to create images for professional environments.
- ****OLE Editing, Object Linking and Embedding**, lets users embed timing diagrams into other publishing programs like Word and FrameMaker. Double clicking on an embedded image launches DataSheet Pro with the selected timing diagram.
- ***Embed an Image or Logo into a diagram** using a text object.

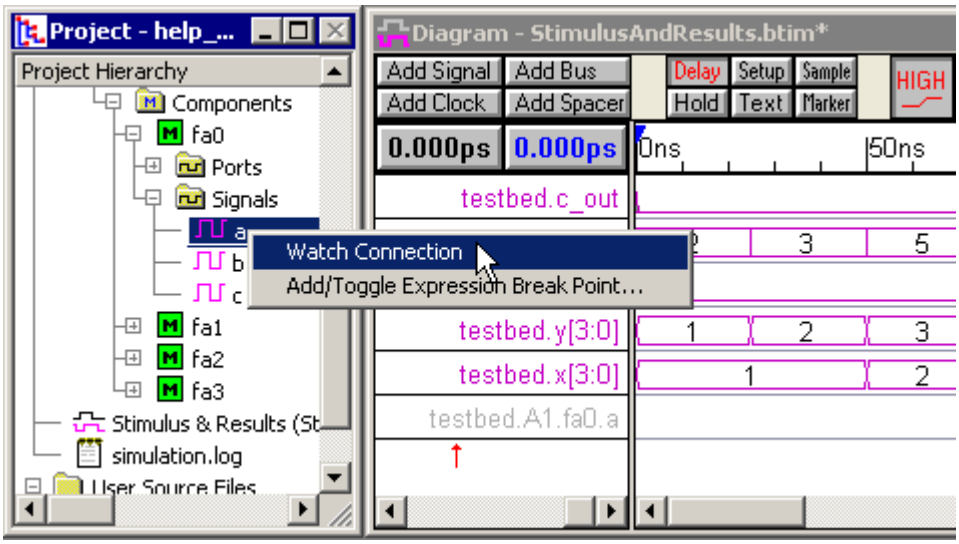


16. VeriLogger Extreme and BugHunter Pro

VeriLogger Extreme is a completely new, high-performance compiled-code Verilog 2001 simulator that significantly reduces simulation debug time.

- VeriLogger Extreme offers fast simulation of both RTL and gate-level simulations with SDF timing information.
- VeriLogger Extreme supports design libraries and design flows for all major ASIC and FPGA vendors, including Actel, Altera, Atmel, LSI Logic, QuickLogic, and Xilinx.
- Includes the BugHunter Pro graphical debugger.
- Includes VeriLogger Pro an interperted IEEE 1364 compliant Verilog simulation engine that supports all major constructs of the language including advanced features such as pin-to-pin timing and PLI interface routines. It is an excellent simulator for RTL level and small FPGA designs, but does not support strengths.

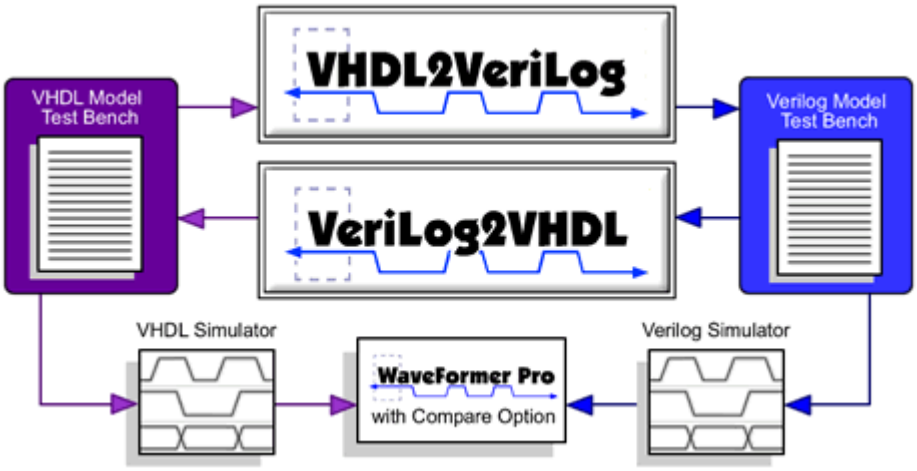
BugHunter uses the SynaptiCAD graphical environment and supports all major HDL simulators. With an integrated debugging environment you can graphically build a project, launch a simulation, and view the results in just a few minutes. The interface also manages the test bench interface so that it is easy to create a set of regression tests to run the design through.



- ***Hierarchical browser** that displays the structural relationships of design modules.
- ***Waveform Viewer** for displaying both simulation results and graphical test benches.
- ***Single step debugging** integrated with the editing environment.
- ***Point-and-click breakpoints**
- ***Graphical and console execution** simulation engines
- ****Unit-Level Test Bench Generation.** If your top-level module has ports, VeriLogger automatically wraps a test bench around the top-level module and creates signals in that test bench to drive and watch the top-level module.

17. Verilog <=> VHDL Translation

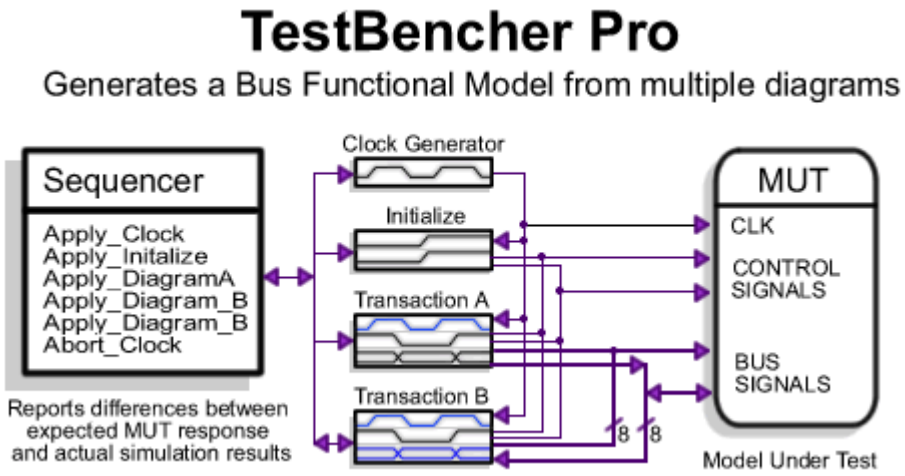
SynaptiCAD offers VHDL2Verilog and Verilog2VHDL, which are command line tools for automatic translation of HDL source code. We have pricing options that include perpetual licenses, yearly licenses, or a daily rate to fit any size translation project. BugHunter Pro can also act as the graphical interface for the translators making it faster to perform the translation-test-tweak cycle.



- **Translation Consulting:** If you have an immediate need to translate some HDL code, we also offer a translation consulting service. With this service, you can get the power and flexibility of our V2V HDL Translators without actually purchasing a license or learning and maintaining the tools.
- Translators support most synthesizable constructs

18. TestBencher Pro Features

TestBencher uses graphical timing diagrams to generate reusable timing transactors (e.g., read cycle, write cycle, interrupt cycle) that can be called by a top-level test bench and applied to the model under test. Reactive Test Bench Option uses a single timing diagram to generate test benches. This chapter covers how to draw signals in a timing diagram, specify state values and clocking domains, verify sequences with sensitive edges, and other waveform related features. The next few chapters cover other graphical elements in the timing diagram such as samples, markers, delays, setups, and holds, and variables and class methods used to define algorithmic functions.



- Uses bus-functional model representation
- Generates native VHDL & Verilog code
- Compatible with all major HDL simulators
- *Resulting code is small and easy to debug
- *Supports both time and cycle-based test benches
- *Supports State and Timing parameter variables
- Set parameters at runtime with function calls
- *Set parameters from data files for regression testing
- *Express runtime-computable timing relationships between signal transitions
- *Built-in timing diagram editor with multiple timing diagram display
- *Simple, orthogonal set of graphical constructs to express transaction protocols:
    - ***Drawn Waveforms:** stimulus and expected response
    - ***State Variables:** parameterize state values
    - ***Delays:** parameterize time delays
    - ***Samples:** verify and react to output from MUT
    - ***Markers:** model looping constructs, insert native HDL subroutine calls, or end transaction
- *Methods provided for waveform generation:
    - Graphically draw stimulus/response waveforms
    - *Generate waveforms using RTL-level equations
    - *Import from simulators: VHDL, Verilog, SPICE

    - *Import from logic analyzers: Agilent, Tektronix
    - *Import state information from spreadsheets
- *Parameterize state values using:
    - Function parameters
    - *File variables
    - *Conditionally control edges using delays. Delays can be time or cycle-based.

- Response Checking with Sample parameters. Sample constructs can monitor and perform actions based on the data sampled.

    - *Two basic versions of samples: Single-Point samples and Windowed samples
    - *Each of these samples can either perform relative to the beginning of the transaction or relative to another event in the diagram.
    - Samples conceptually model IF-THEN-ELSE code.
    - Default actions are provided which perform basic logging and error detection
    - *Actions can be added to the interface using native language code segments
    - *Samples can conditionally monitor a sequence of events
    - ***Sample actions can trigger delayed state transitions and other samples. These triggered events can be chained.

- *File associations allow simulation data to be read from and written to files

    - *Input state values
    - *Output sampled state values
    - *Input data from a file that can be accessed randomly for use during simulation

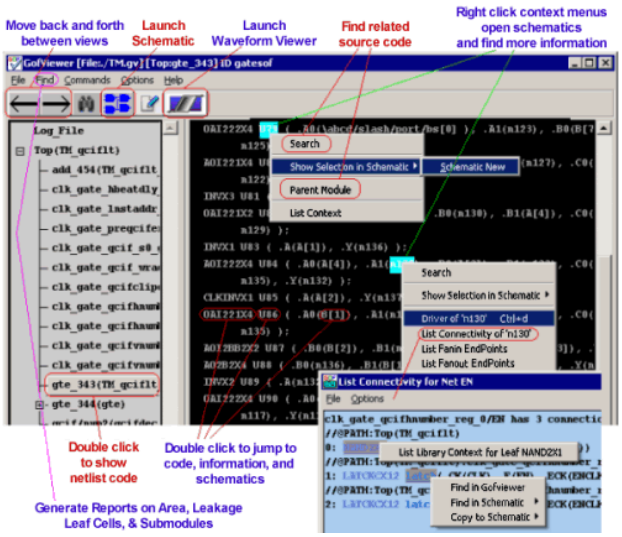
- ***Transaction Manager** that can take lists of transactions from files, transactions applied by other interface models, and randomly generated transaction and apply them to the model under test.
- **External Simulator Control:** TestBencher Pro can control external simulators through it's graphical interface, so that compilation and simulation of the project can be handled without having to exit TestBencher. This is particularly useful when multiple tools are needed to compile and simulate a project. For example, if you are using one of the new verification languages you will need a tool to compile the test bench into either a dynamically linked library or byte code. You will also need a VHDL or Verilog simulator and a make file containing all of the information about your model under test and the commands to dynamically link to the test bench library. With TestBencher, all of these details are automatically handled for you. TestBencher stores information about both your simulator and verification compiler and can remotely call those programs and display the results of the simulation. Supports the following simulators:

    - Aldec Active_HDL
    - Cadence NC Verilog, NC VHDL, & Verilog XL
    - GNU gcc
    - Microsoft C++ Compiler
    - Model Sim GUI & Command Line
    - SynaptiCAD's VeriLogger Pro
    - Synopsys VCS & Scirocco
    - Synopsys VERA
    - Verisity Specman Elite

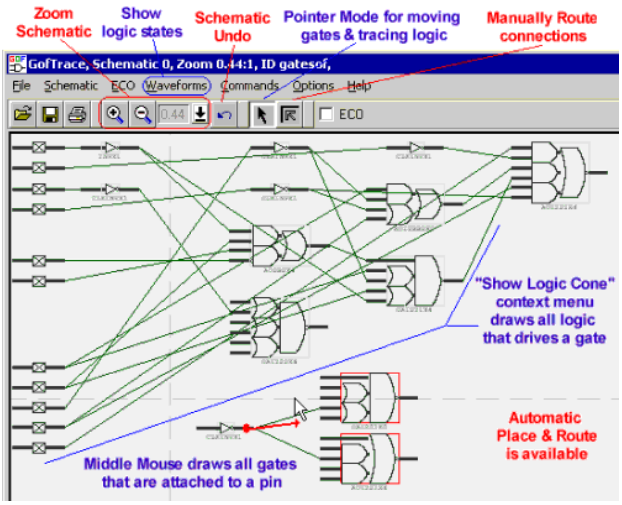
19. Gates-on-the-Fly

Gates-on-the-Fly (GOF) graphically analyzes and edits large Verilog netlists that have been generated from a synthesis or layout tool. Netlists sometimes require changes to either meet timing closure specifications, fix functional logic bugs, or to repartition a design. Using GOF, you can easily find and view specific logic cones in your design on a schematic to visualize just the paths you need to see without unnecessary clutter. GOF also simplifies mapping from RTL level constructs to their gate-level equivalents, so that you can pinpoint the locations where changes need to be made. GOF's ECO mode supports both graphical and script-based editing features for tracking ECO changes. Metal-only ECO operations are also supported with an automatic spare gates flow.

- Locate Sections of interest in the design in GofViewer which displays a netlist as a hierarchical tree of module instances with an associated text window.
- Fully interactive and incremental schematic generator
- Natural gate symbol display without requiring an additional symbol file
- Graphical mode for perfoming netlist ECOs



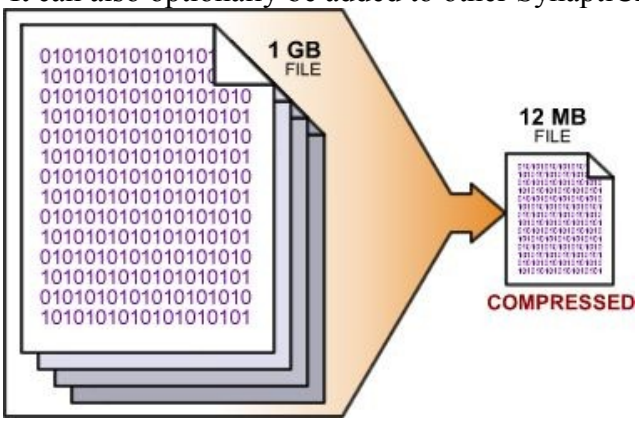
- Script based ECOs using a powerful API that does much more than other TCL based scripts
- Netlist to RTL wire matching feature to help easily locate the point to perform an ECO
- A programming interface to process netlists
- GOF can display timing violations from Prime Time report files graphically on a schematic
- Logic Cone ECO script that changes the entire logic cone that drives an input pin and replaces it with a new set of logic from a newly re-synthesized netlist
- ECO edit session results can be saved in several formats



- Lots of other built-in netlist operations, informational reports, and utilities.

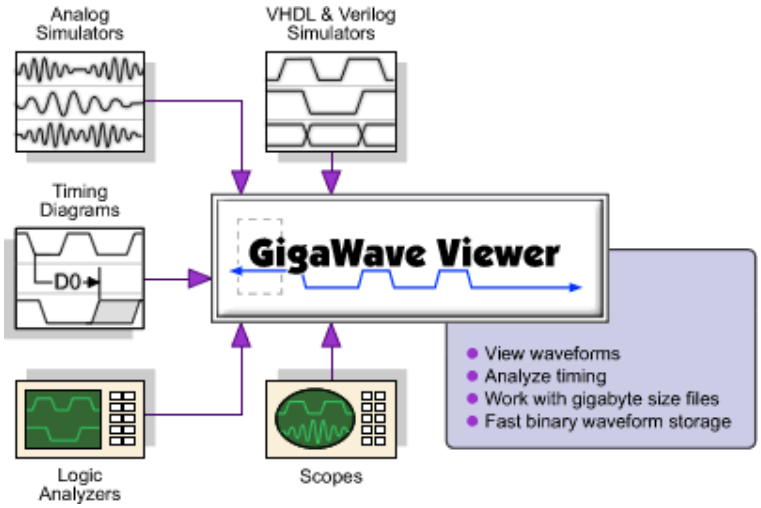
20. GigaWave Option & Viewer Features

GigaWave File support option allows SynaptiCAD's products to view and edit very large simulation and logic analyzer waveform files. The ability to edit and annotate large waveform files is a unique feature of the SynaptiCAD product line that is not offered by any other product on the market. The GigaWave options uses several advanced waveform compression algorithms and a high-speed, binary waveform database that lets the program load, edit, and compare files that are 200 times bigger than can normally be handled on a given system. The GigaWave file support option is a "must-have" feature for engineers who need to view, edit, or compare large sets of waveform data. GigaWave is included in GigaWave Viewer and in the G-Series products. It can also optionally be added to other SynaptiCAD products.



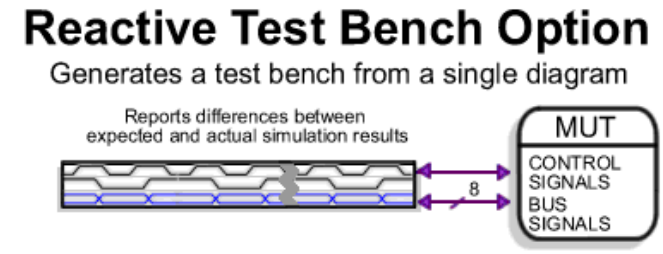
Gigawave Viewer combines SynaptiCAD's WaveViewer with our high-performance gigawave compression engine to create the lowest cost waveform viewer capable of handling multi-gigabyte VCD files.

- Includes a PLI-based library that can be integrated with your favorite simulator to generate highly compressed BTIM files. Using BTIM waveform dumping can speed up simulation by up to 3x over dumping using an ordinary VCD dump and the resulting files are generally 100x smaller.
- BTIM files also load much faster than VCD files (typically around 500x faster)! GigaWave also loads SPICE results, TDML, logic analyzer data, and more.
- Batch Mode Operation



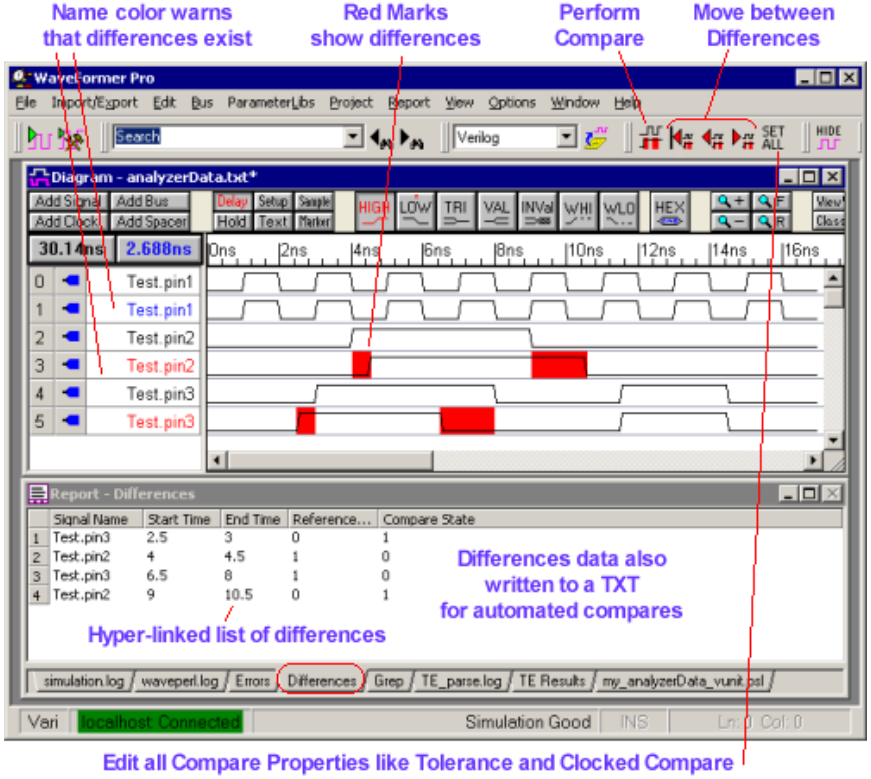
21. Reactive Test Bench Generation Option

The Reactive Test Bench Generation Option bridges the gap between the stimulus waveform test benches that are native to most of the SynaptiCAD product line and the bus-functional model generation of TestBencher Pro. This option allows users to describe single timing diagram test benches that react to the model under test and generate pass/fail reports. The Reactive Test Bench Generation Option can be added to WaveFormer Pro, WaveFormer Lite, DataSheet Pro, VeriLogger, and BugHunter Pro.



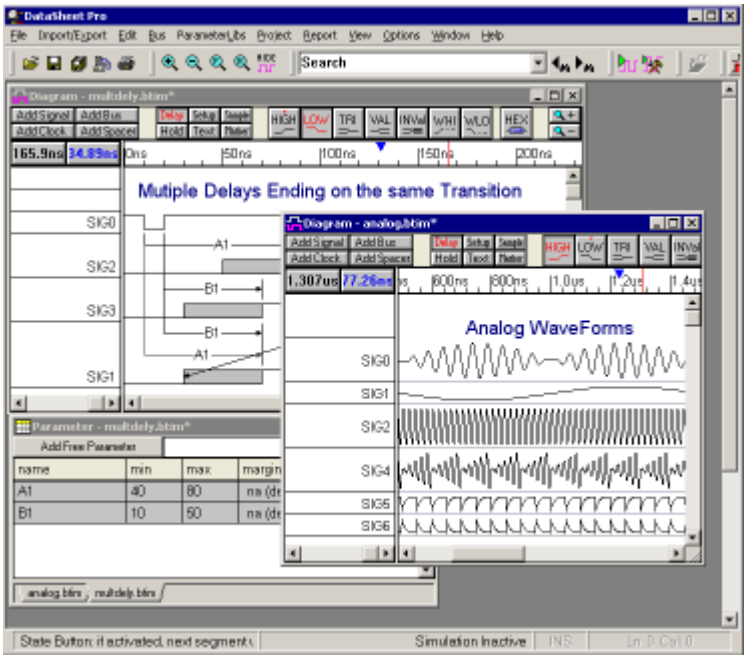
22. WaveFormer Comparison Option

Waveform comparison is an optional feature and all of the SynaptiCAD timing diagram editors and graphical products can be upgraded to include these features. The Waveform Comparison feature graphically displays the differences between waveforms for two timing diagrams or individual signals. This feature is especially useful when comparing two different simulation runs, as well as for comparing logic analyzer data to a simulation run. Differences are shown as red regions on the compare signal. There are settings for tolerance regions and clocked compares to help filter out unimportant differences.



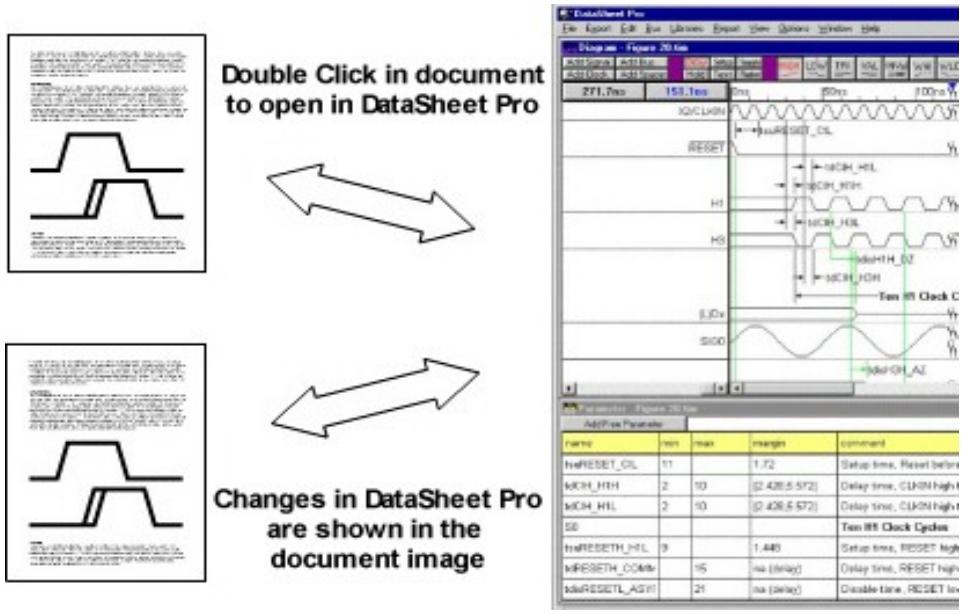
23. Multiple Timing Diagram Option

Multiple Timing Diagram Window option allows more than one timing diagram to be opened at the same time. This feature is extremely useful for visually comparing different timing diagrams. With this feature you can view one timing diagram while drawing a similar timing diagram in the design. Also view timing diagrams and simulation results at the same time. The multiple parameter tables are shown as different tabs in the Parameter window. As you switch between diagrams the Parameter window shows parameters for the selected timing diagram. This feature comes standard with TestBencher Pro and DataSheet Pro and is an optional feature for our other software products.



24. OLE Option

The OLE option allows images to be embeded into word processors and other applications so that the image and the timing diagram file are linked. Double clicking on the image will launch the timing diagram editor for editing. DataSheet Pro includes the OLE option, and it is also available as an option to WaveFormer Pro, Timing Diagrammer Pro, VeriLogger, BugHunter and TestBencher Pro. This is a Windows Only Feature.



OLE provides a convenient way to manage timing diagrams which are included in many of your documents, such as word processor files, spreadsheets, and presentation graphics. Then, when you make changes to your timing diagrams, they are automatically updated in the linked or embedded third-party files. This feature greatly simplifies documentation by allowing changes to timing diagrams to be made in only one place.

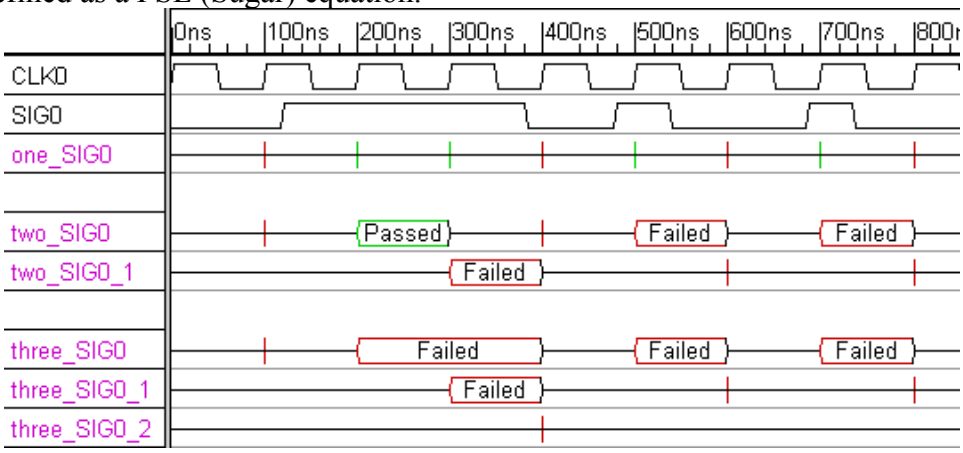
25. Timing Analysis Option

SynatiCAD's timing analysis engine uses sophisticated algorithms to detect both timing violations and overly pessimistic assumptions about system performance. The timing analysis engine accounts for timing effects that are difficult to compute manually such as delay correlation, reconvergent fan-out, and jitter and buffering in clock trees. The timing analysis engine comes standard with WaveFormer Pro, Timing Diagrammer Pro, and DataSheet Pro. It can also be purchased as an option to upgrade the waveform editor in VeriLogger Pro, BugHunter Pro, or WaveFormer Lite.

- Reconvergent Fanout (Common Delay Removal)
- Delay Correlation (Skew Removal)
- Clock Timing (Jitter and Clock Buffer Delay)

26. Transaction Tracker Option

The Transaction Tracker Option displays areas in a waveform file that match a transaction pattern defined as a PSL (Sugar) equation.



27. Software Support

We offer free telephone and email technical support to our customers. All members of our technical support staff are experienced digital engineers and are very familiar with the product's operation. Bug reports are our highest priority, and we deliver bug fixes as quickly as possible.

28. Platform Support

We currently offer native binary support for the following operating systems:

- All Windows platforms
- Most major Linux platforms
- SunOS, Solaris and HP-UX

29. Upgrade Path

Because SynaptiCAD's products are written from the ground up in C++ we are able to add new features much more rapidly than most software companies. So please call us for a feature request. (Many of our best features are a direct response to customer requests).